CN0363

ANALOG DEVICES

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CN0363

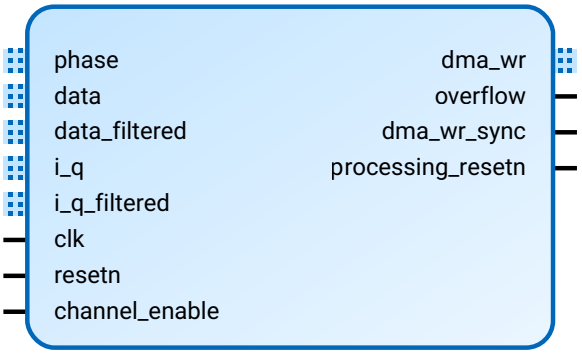
CN0363 library comprises two IPs:

- CN0363 DMA Sequencer
- CN0363 Phase Data Sync

CN0363 DMA Sequencer core acts as a link between the CN0363 processing pipeline and the connected DMA controller. CN0363 Phase Data Sync assembles the raw ADC sample data into a 24-bit word and convert it to two's complement.

CN0363 DMA Sequencer

The CN0363 Sequencer FPGA Peripheral is part of the CN0363 HDL project and is responsible to sequence the various data channels to the DMA.



cn0363_dma_sequencer

Files

Name	Description
library/cn0363/cn0363_dma_sequencer/cn0363_dma_sequencer.v	Verilog source for the peripheral.
library/cn0363/cn0363_dma_sequencer/cn0363_dma_sequencer_ip.tcl	TCL script to generate the Vivado IP-integrator project for the peripheral.

Signal and Interface Pins

phase
AXI-Stream slave - Phase data channel.

Physical Port	Logical Port	Direction	Dependency
phase_valid	TVALID	in	
phase_ready	TREADY	out	
phase	TDATA	in [31:0]	

data
AXI-Stream slave - Sample data channel.

Physical Port	Logical Port	Direction	Dependency
data_valid	TVALID	in	
data_ready	TREADY	out	

Physical Port	Logical Port	Direction	Dependency
data	TDATA	in [23:0]	

data_filtered
AXI-Stream slave - Filtered sample data channel.

Physical Port	Logical Port	Direction	Dependency
data_filtered_valid	TVALID	in	
data_filtered_ready	TREADY	out	
data_filtered	TDATA	in [31:0]	

i_q
AXI-Stream slave - Demodulated I/Q sample data channel.

Physical Port	Logical Port	Direction	Dependency
i_q_valid	TVALID	in	
i_q_ready	TREADY	out	
i_q	TDATA	in [31:0]	

i_q_filtered
AXI-Stream slave - Filtered demodulated I/Q sample data channel.

Physical Port	Logical Port	Direction	Dependency
i_q_filtered_valid	TVALID	in	
i_q_filtered_ready	TREADY	out	
i_q_filtered	TDATA	in [31:0]	

dma_wr
FIFO Write Interface master - Low-level SPI bus interface that is controlled by peripheral.

Physical Port	Logical Port	Direction	Dependency
dma_wr_en	EN	out	
dma_wr_data	DATA	out [31:0]	
dma_wr_overflow	OVERFLOW	in	
dma_wr_xfer_req	XFER_REQ	in	

Ports

Physical Port	Direction	Dependency	Description

Physical Port	Direction	Dependency	Description
`clk`	in		Clock - All other signals are synchronous to this clock. Bus `phase_data_data_filtered_i_q_i_q_filtered_dma_wr` synchronous to this clock domain.
`resetn`	in		Synchronous active low reset - Resets the internal state machine of the core.
`overflow`	out		Output - The overflow signal is asserted if a overflow on the DMA interface is detected.
`dma_wr_sync`	out		
`channel_enable`	in [13:0]		Input - Data channel enable sequencer output enable.
`processing_resetn`	out		Output - Reset signal for the processing pipeline Bus `phase_data_data_filtered_i_q_i_q_filtered_dma_wr` synchronous to this reset signal.

Theory of Operation

The CN0363 DMA sequencer core acts as a link between the CN0363 processing pipeline and the connected DMA controller. On one side it accepts data from the processing pipeline and on the other side it sends the data to the DMA controller. The core is only active when the DMA controller signals that it is waiting for data, when it is inactive it also asserts the `processing_resetn` signal to keep the processing pipeline in reset. Since the DMA is running at a much faster clock than the output data rate from the processing pipeline the different channels are time-division-multiplexed and send one by one to the DMA controller over the `dma_wr` interface.

When active the core cycles through the input channels in the following order.

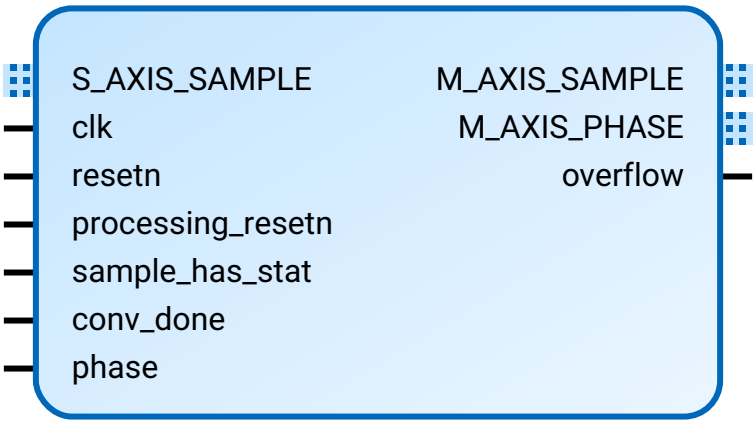
1. phase (Reference channel)
2. data (Reference channel)
3. data_filtered (Reference channel)
4. i_q, I component (Reference channel)
5. i_q, Q component (Reference channel)
6. i_q_filtered, I component (Reference channel)
7. i_q_filtered, Q component (Reference channel)
8. phase (Sample channel)
9. data (Sample channel)
10. data_filtered (Sample channel)
11. i_q, I component (Sample channel)
12. i_q, Q component (Sample channel)
13. i_q_filtered, I component (Sample channel)
14. i_q_filtered, Q component (Sample channel)

Each of these has a corresponding bit in the `channel_enable` and only if the bit is set the channel is sent to the `dma_wr` interface, otherwise it is discarded. This allows an application to select which data channels it wants to capture.

More Information

- CN0363 HDL project

CN0363 Phase Data Sync



cn0363_phase_data_sync

The CN0363 Phase Data Sync FPGA Peripheral is part of the EVAL-CN0363-PMDZ HDL reference design and is responsible for preparing the ADC conversion result data and aligning it with the phase and feeding both to the processing pipeline.

Files

Name	Description
/library/cn0363/cn0363_phase_data_sync/cn0363_phase_data_sync.v	Verilog source for the peripheral.
/library/cn0363/cn0363_phase_data_sync/cn0363_phase_data_sync_ip.tcl	TCL script to generate the Vivado IP-integrator project for the peripheral.

Signal and Interface Pins

S_AXIS_SAMPLE
AXI-Stream slave - Input sample data stream

Physical Port	Logical Port	Direction	Dependency
`s_axis_sample_valid`	`TVALID`	in	
`s_axis_sample_ready`	`TREADY`	out	
`s_axis_sample_data`	`TDATA`	in [7:0]	

M_AXIS_SAMPLE
AXI-Stream master - Output sample data stream

Physical Port	Logical Port	Direction	Dependency

Physical Port	Logical Port	Direction	Dependency
m_axis_sample_valid	TVALID	out	
m_axis_sample_ready	TREADY	in	
m_axis_sample_data	TDATA	out [23:0]	

M_AXIS_PHASE

AXI-Stream master - Output phase data stream

Physical Port	Logical Port	Direction	Dependency
m_axis_phase_valid	TVALID	out	
m_axis_phase_ready	TREADY	in	
m_axis_phase_data	TDATA	out [31:0]	

Ports

Physical Port	Direction	Dependency	Description
clk	in		Clock - All other signals are synchronous to this clock. Bus S_AXIS_SAMPLE_M_AXIS_SAMPLE_M_AXIS_PHASE is synchronous to this clock domain.
resetn	in		Synchronous active low reset - Resets the internal state machine of the core. Bus S_AXIS_SAMPLE_M_AXIS_SAMPLE_M_AXIS_PHASE is synchronous to this reset signal.
processing_resetn	in		Synchronous active low reset - Indicator that the processing pipeline is in reset.
sample_has_stat	in		Input - Whether the incoming data on S_AXIS_SAMPLE has the STAT register appended.
conv_done	in		Input - Conversion done signal from the ADC.
phase	in [31:0]		Input - Current excitation signal phase.
overflow	out		Input - The overflow signal is asserted if a new sample arrives before the previous one has been consumed.

Theory of Operation

The CN0363 Phase Data Sync FPGA Peripheral takes the raw ADC sample data read by a SPI controller from the ADC on the S_AXIS_SAMPLE stream. The data is assembled into 24-bit word and converted from offset binary to two's complement signed.

When a rising edge is detected on the conv_done signal the core takes a snapshot of the phase input signal. This data will be assumed to the phase that belongs to the next incoming data sample on the S_AXIS_SAMPLE.

The data is aligned with the corresponding phase data and both are send out on the `M_AXIS_SAMPLE` and `M_AXIS_PHASE stream`.

If the `sample_has_stat` signal is asserted the core will receive 32-bit instead of 24-bit per sample on the S_AXIS_SAMPLE stream. The last 8-bit are assumed to contain the STAT register of the ADC, which among other things contains the information about which channel the ADC result belongs to. This information can be used to detect and fix channel swaps. If `sample_has_stat` is not asserted the core assumes that no channel swaps happen and the whole pipeline is always running fast enough to accept a sample before the next one is ready.

If `processing_resetn` is asserted the processing pipeline is assumed to be in reset and incapable of accepting new samples and when a new sample arrives at the `S_AXIS_SAMPLE` port a overflow condition is generated. The signal also resets the channel swap detection logic and makes sure that the next sample that is inserted into the processing pipeline after the reset belongs to the first channel.

More Information

- CN0363 HDL project