Bridge of Life Education

Full Stack IC (fsic) Designer Development

3rd meeting, 3/6/2023

Jiin Lai

Agenda

1. Caravel Block Diagram & Interface
2. Caravel Documents & Study Topics
3. Caravel SOC Test-bench and Firmware - Kevin
4. Q & A

Poll

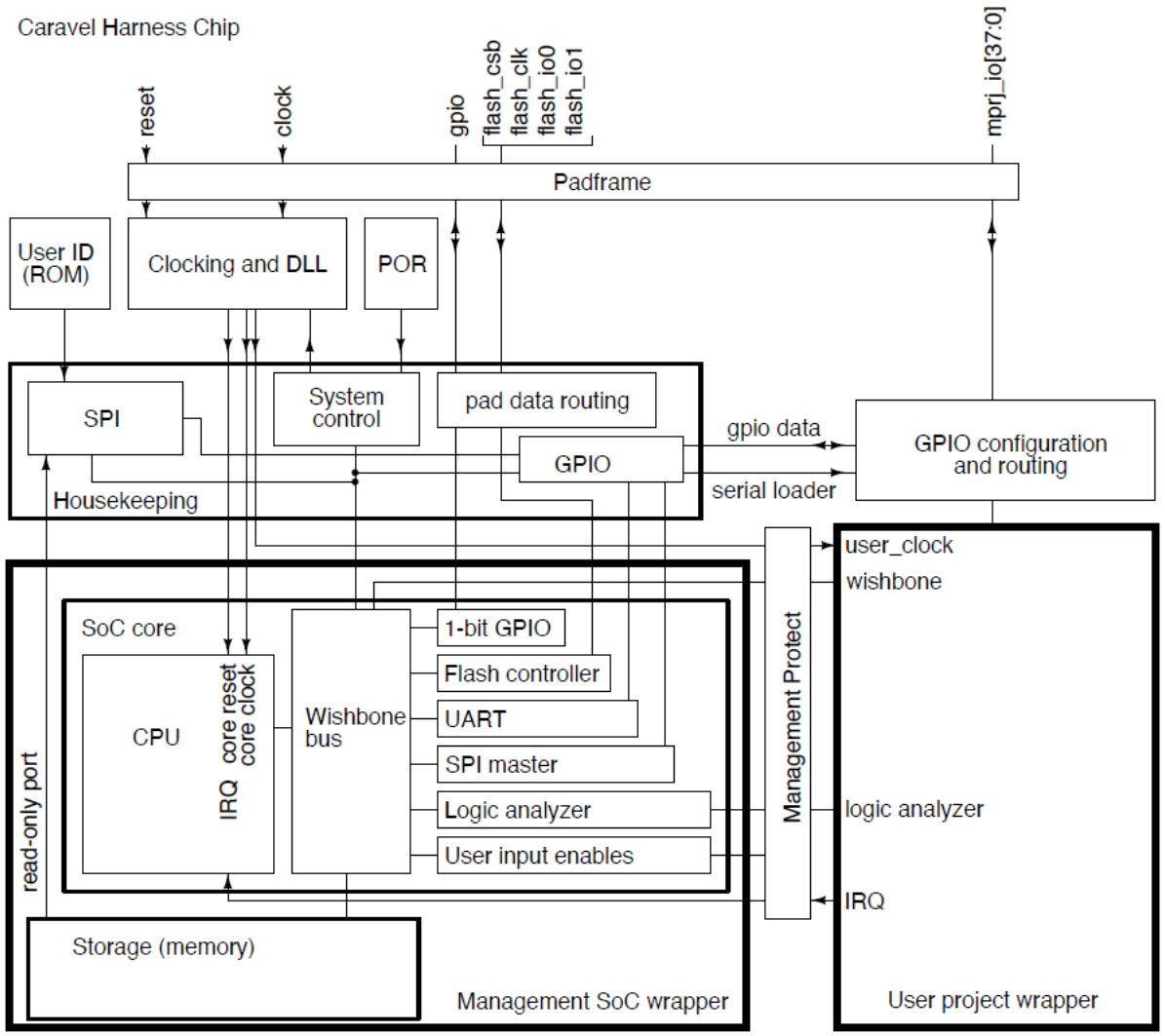
- iverilog/gtkwave/vtags installation and running ?
  - https://github.com/bol-edu/caravel-soc
- Try to verify gcd example ?
  - https://github.com/bol-edu/caravel-lab/blob/main/README.md#1-custom-rtl-design
- Verilog Introduction document ?
  - Berkeley EE151 Verilog: https://drive.google.com/drive/folders/1QnqOhnsTvAckKUsZwyz48KgyCQVNwdAy?usp=share_link
  - NTU CVSD Verilog https://drive.google.com/drive/folders/1AGHvs2fLISm-4GthBTgfLKU6qJQVt8qA?usp=share_link

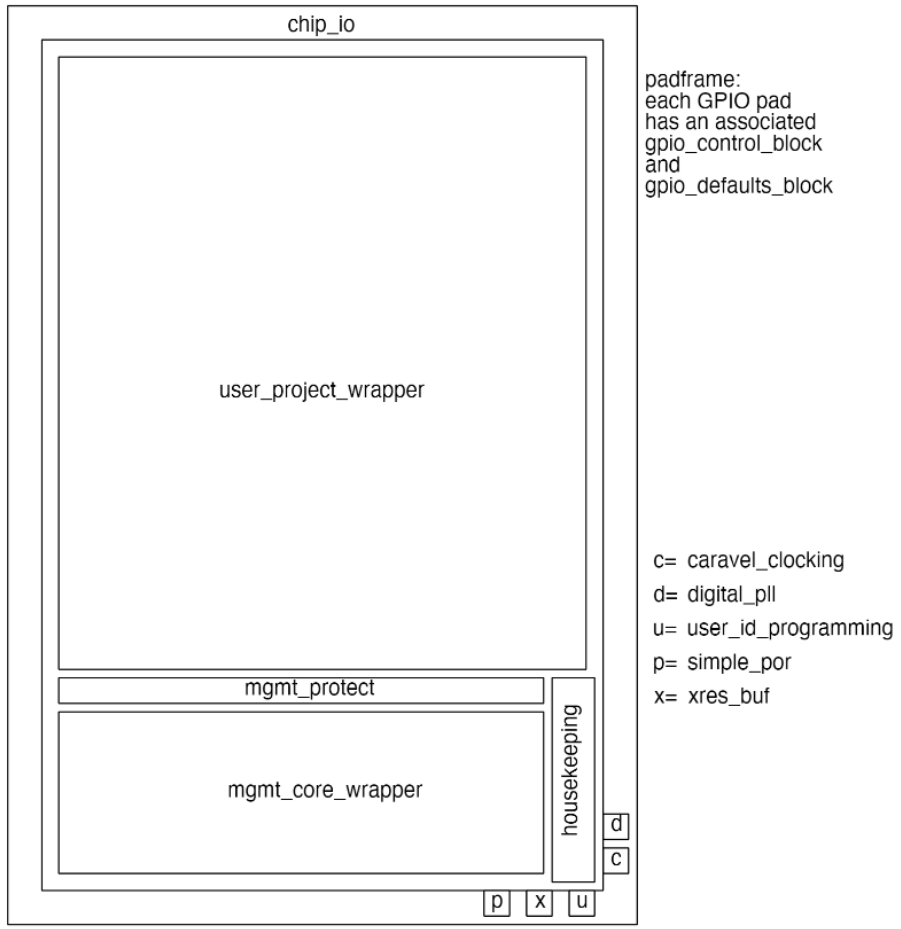
Verilog Coding Style

- Verilog Coding Style:
  http://www.ee.ncu.edu.tw/~jfli/vlsidi/lecture/VerilogCoding-2009.pdf
- Verilog Naming Rule
  https://github.com/lowRISC/style-guides/blob/master/VerilogCodingStyle.md
  Condensed version: https://github.com/lowRISC/style-guides/blob/master/VerilogCodingStyle.md#appendix---condensed-style-guide

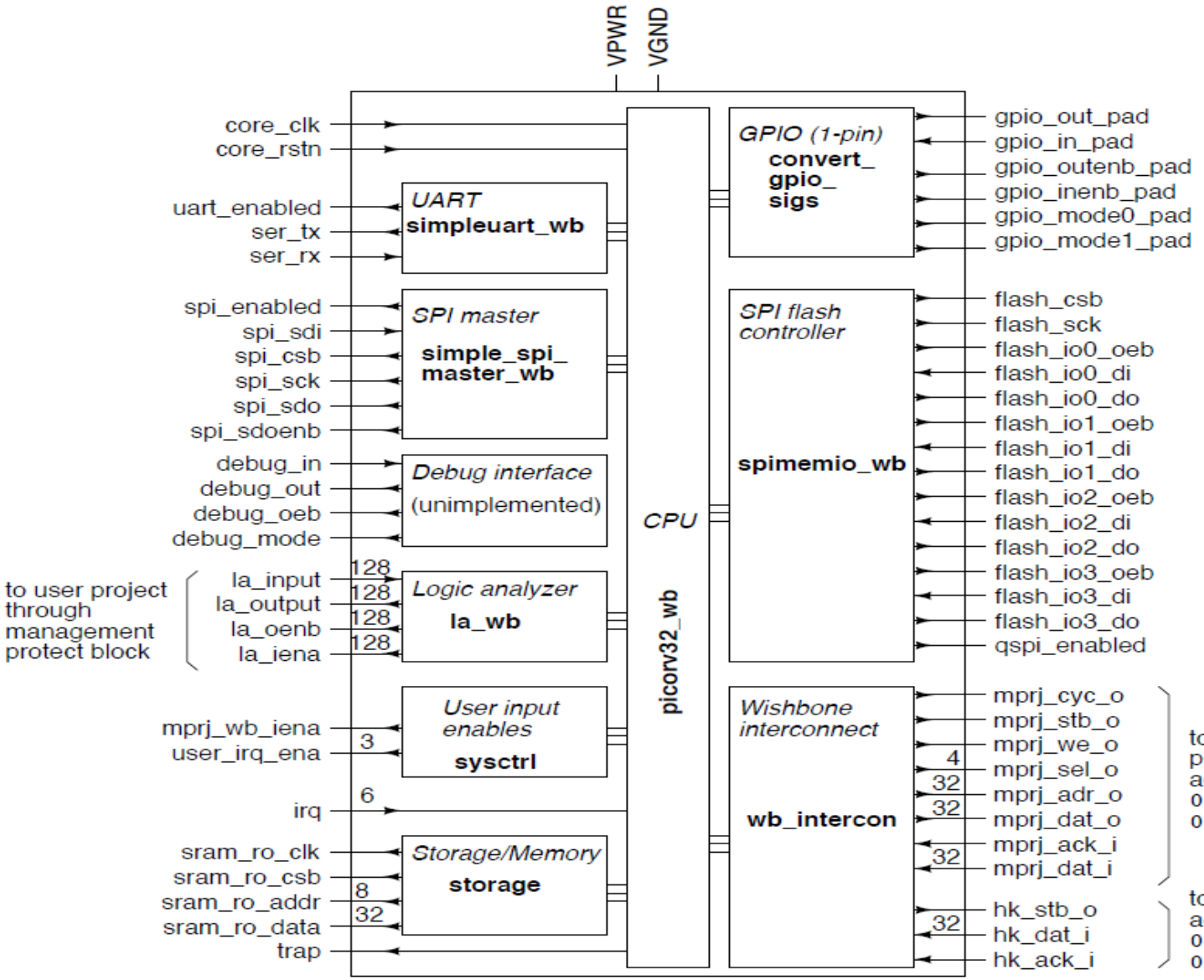
Caravel Block Diagram & Interface

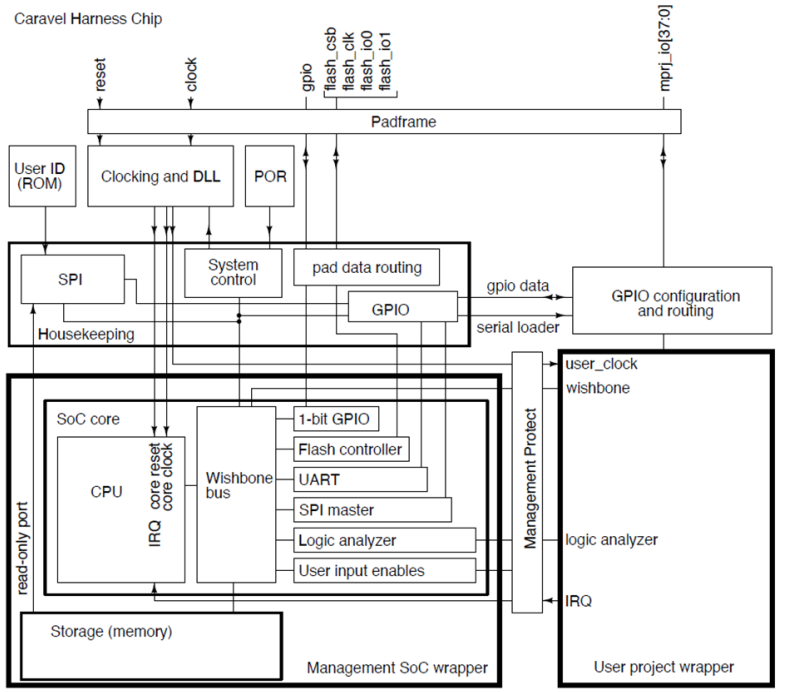
Caravel Block Diagram



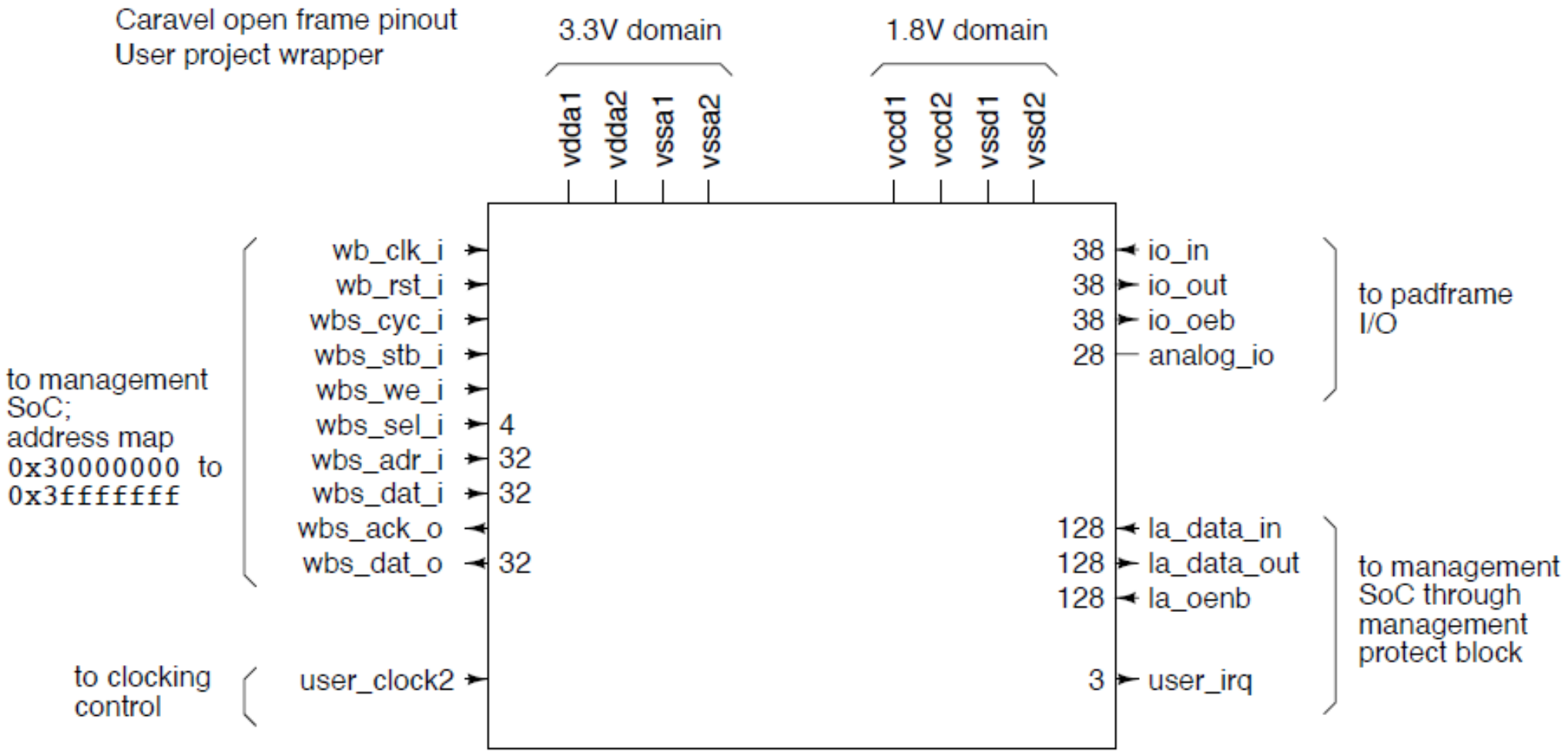


Caravel open frame pinout
Management core wrapper

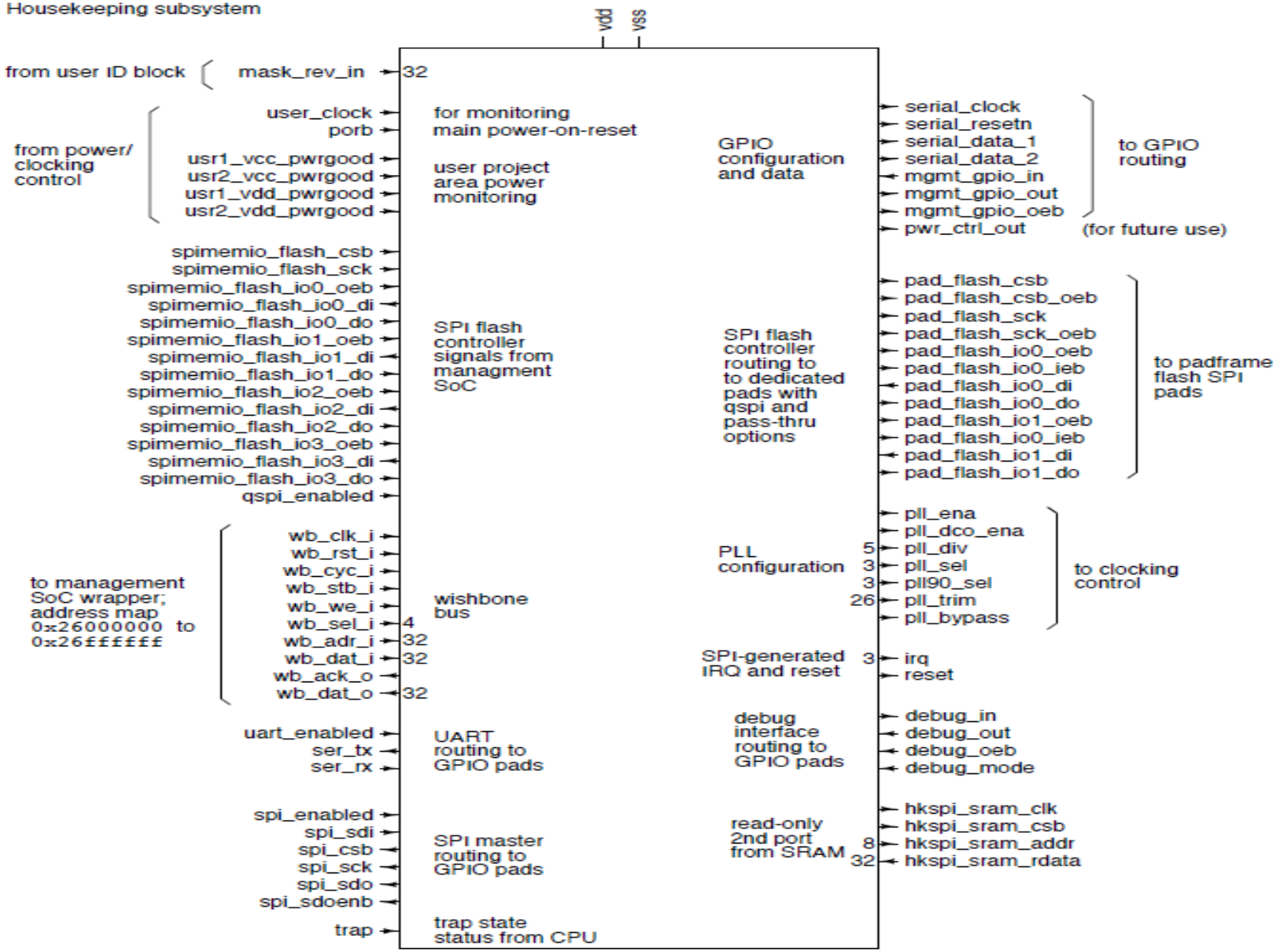




All signals connect to the housekeeping subsystem unless otherwise specified.
Internal block names shown in boldface are for the **caravel-pico** implementation.


Caravel open frame pinout
User project wrapper
3.3V domain
1.8V domain
vdda1
vdda2
vssa1
vssa2
vccd1
vccd2
vssd1
vssd2
to management SoC; address map 0x30000000 to 0x3fffffff
wb_clk_i
wb_rst_i
wbs_cyc_i
wbs_stb_i
wbs_we_i
wbs_sel_i 4
wbs_adr_i 32
wbs_dat_i 32
wbs_ack_o
wbs_dat_o 32
to clocking control
user_clock2
38 io_in
38 io_out
38 io_oeb
28 analog_io
to padframe I/O
128 la_data_in
128 la_data_out
128 la_oenb
3 user_irq
to management SoC through management protect block

Caravel open frame pinout
Housekeeping subsystem



All signals connect to the management SoC wrapper unless otherwise specified.

Caravel SOC Documents

- Caravel Datasheet:
  - https://raw.githubusercontent.com/milovanovic/caravel_spectrometer/master/doc/caravel_datasheet.pdf
- Document Github:
  - https://github.com/efabless/caravel/tree/main/docs

caravel / docs / rst /

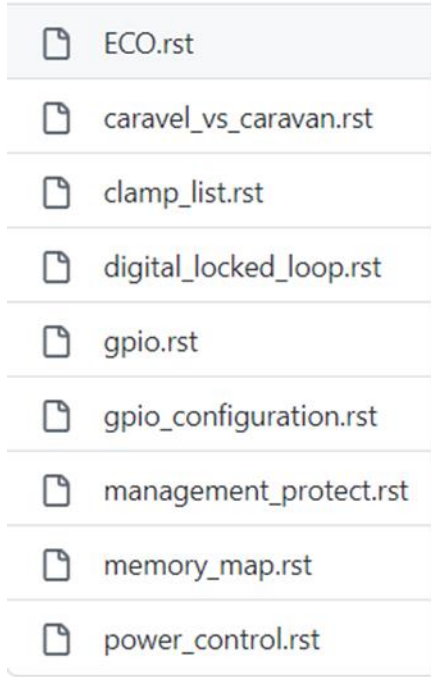
- ECO.rst
- caravel_vs_caravan.rst
- clamp_list.rst
- digital_locked_loop.rst
- gpio.rst
- gpio_configuration.rst
- management_protect.rst
- memory_map.rst
- power_control.rst

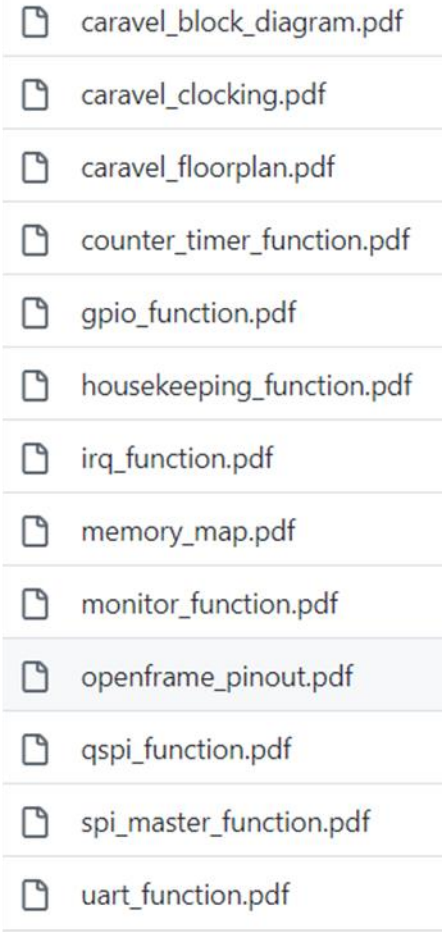
caravel / docs / pdf /

- caravel_block_diagram.pdf
- caravel_clocking.pdf
- caravel_floorplan.pdf
- counter_timer_function.pdf
- gpio_function.pdf
- housekeeping_function.pdf
- irq_function.pdf
- memory_map.pdf
- monitor_function.pdf
- openframe_pinout.pdf
- qspi_function.pdf
- spi_master_function.pdf
- uart_function.pdf

Caravel SOC Design Study Topics

- Top level: - caravel
  - Clocking
  - Digital_locked_loop
  - Management_protect
  - Power_control
  - IO pads
  - Clamp
- Memory map: memory_map.pdf - caravel
- HouseKeeping - caravel-ip
  - Housekeeping_function
  - qspi,
  - spi,
  - uart,
  - irq,
  - debugging,
  - mprj io
  - Counter timer
  - Monitor_function
- Management Core - caravel-ip
  - Wishbone bus
  - Logic analyzer, storage





Suggested Study Method

- Study document (Caravel), device specification, e.g. uart, spi, flash …
- Study related rtl code
- Develop test vector (riscv code / test-bench) & run simulation
- Cross-reference among: document, verilog code, simulation waveform

Presentation in the following two weeks

Bridge of Life Education

Caravel SoC Testbench and Firmware

2023/03/06

Next

- Study System Operation Paths
- Develop an FIR to exercise
  - FIR axis, axim interface
  - FIR data input by Wishbone, LA, GPIO
  - Develop RISC-V code, Verilog test-bench (Streaming)