Bridge of Life Education

Full Stack IC (fsic) Designer Development

3/1/2023

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Agenda

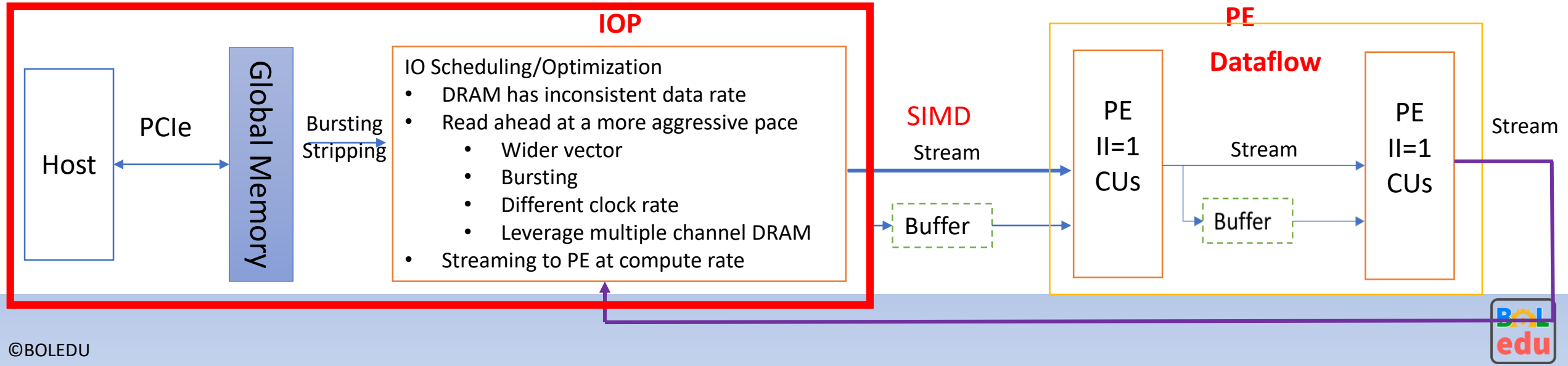
1. Proposed Accelerator Architecture Framework
2. FSIC Validation Architecture
3. Development Milestones
4. Project Execution Logistics

We will name the project FSIC (means: Full-Stack IC)

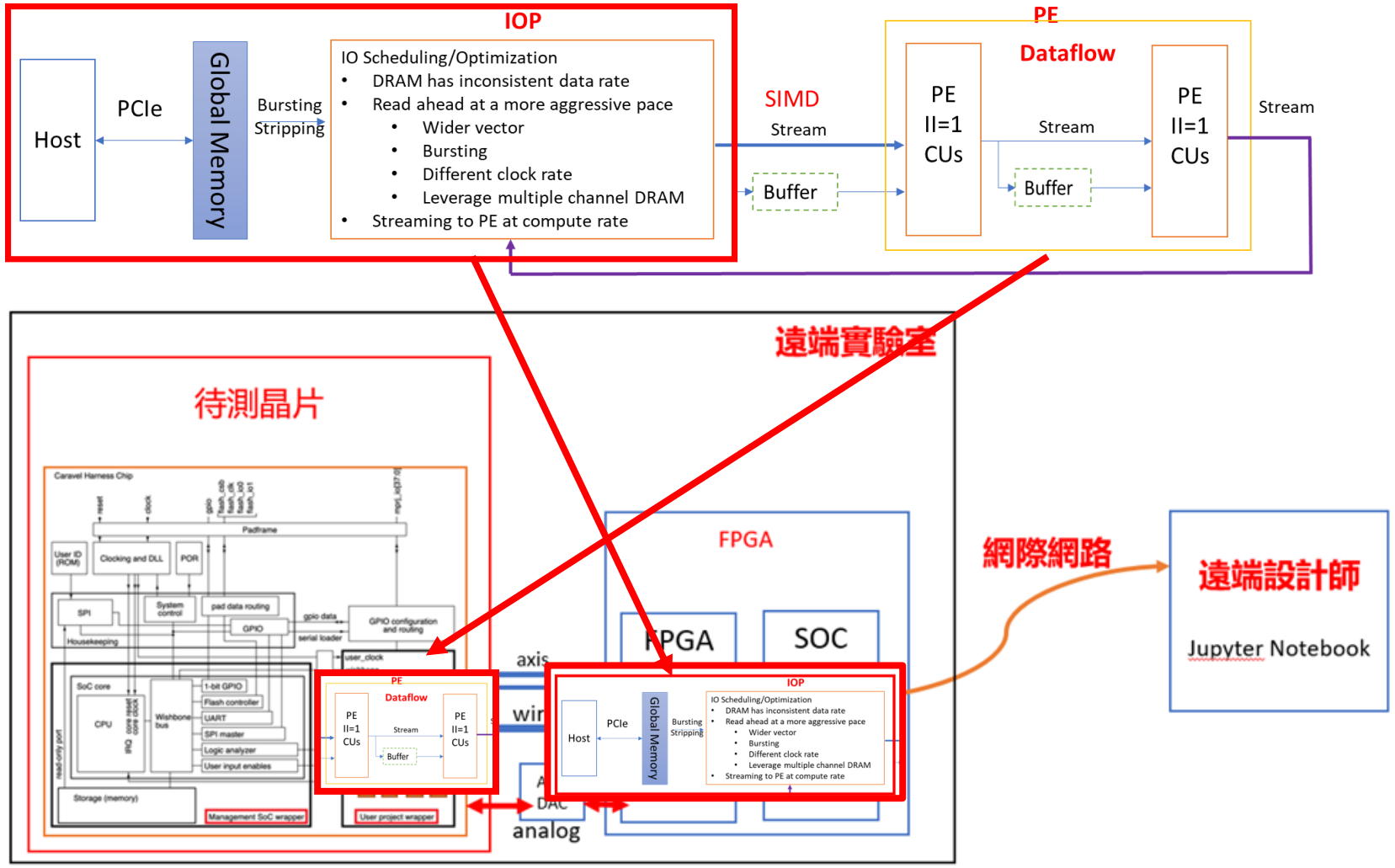
User Project Development Platform

A Proposed Accelerator Architecture Framework

- Separate data movement (IOP) from Computation (PE)
- Optimize data movement first – use pseudo-design PE with II = 1
- Memory access extraction/transformation/optimization (**Polyhedral Analysis**)
- Streaming with Buffering/Cache for non-sequential access, e.g. window/line buffers
- Processing Stage (PE)
  - Multiple CUs (degree of folding, maximize data bandwidth SIMD)
  - Pipeline within PE (II = 1)
  - Dataflow among PEs
  - Systolic Array (Pipeline + Dataflow) - connectivity
- Design for Scalability (parameterized)



IC Validation System Block Diagram



FPGA

1. Memory, IO Access function, includes memory access extraction/transformation/optimization (Polyhedral Analysis). Note: it can be an evolutionary optimization process. FPGA provides the benefit of reprogramming when a new idea comes up.
2. It provides necessary memory buffers.
3. Part of kernel processing can be moved to the FPGA side o reduce the area of the Caravel chip.
4. Provide data to kernel processing system through stream interface (axis)
5. Kernel-specific test-bench code implemented in FPGA hardware (through direct wires)

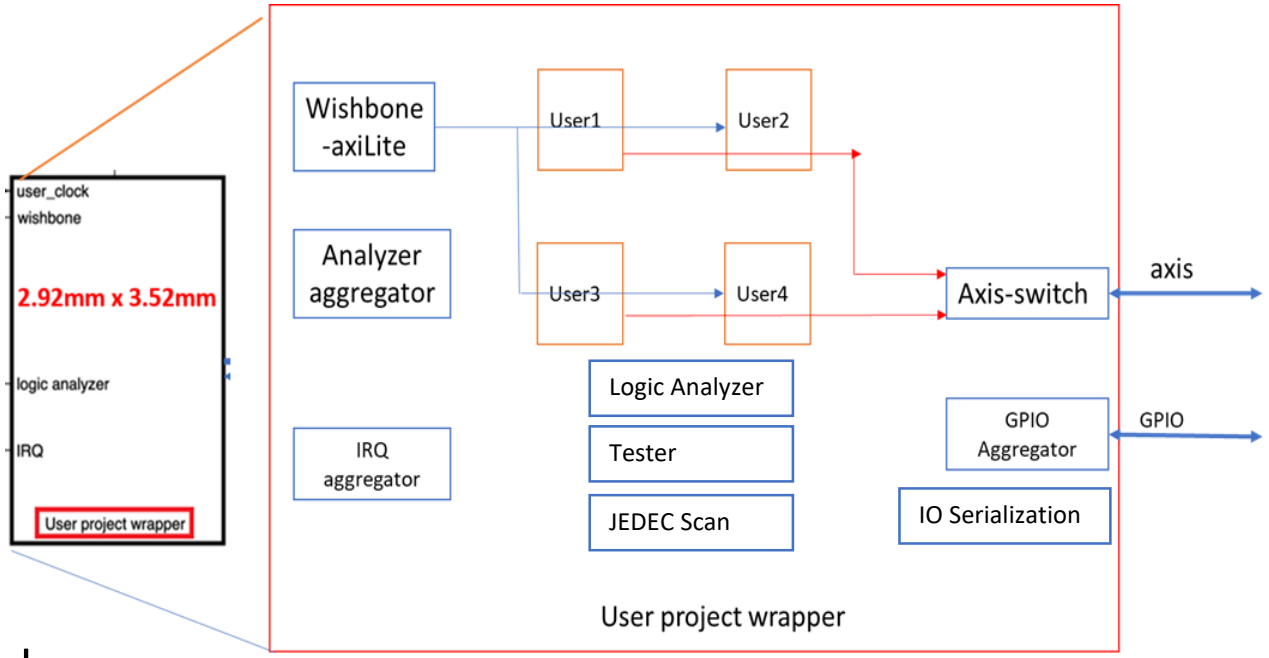
Caravel Chip

1. User Project (Kernel processing) interface with FPGA through stream (axis) interface or direct wires （GPIO pins）
2. Dataflow architecture for IP development
3. Build in debugging facilities, e.g., logic analyzer, tester, JEDEC controller for ATPG

FSIC Validation Architecture

Testing Function in Caravel Chip

1. Aggregator/Dis-aggregator for
   1. Module: Wishbone-to-axilite (wishbone2axilite)
   2. Module: GPIO
   3. Module: INTC
   4. Module: AXIS-switch - AXIS interface
2. Logic analyzer
   1. Programmable trigger condition
   2. Data logger and compressed
   3. Compressed data sent to FPGA through axis interface
3. Tester
   1. Programmed Sequencer
   2. Signal conditioning
4. JEDEC – for scan-chain (ATPG)
5. IO serialization – increase # of pins by ratio-down core clock, e.g. IO clock = 10 x core clock



Testing Function in FPGA

1. Reset sequence control
2. Caravel firmware downloader
3. Memory-AXIS DMA (Send & Receive)
4. Direct wires on GPIO (through hardware or mcu-control)
5. IO Serialization

System Initialization Sequence

1. Reset Exit Sequence : FPGA -> Caravel
    1. FPGA GPIO output (default: assert to reset) to control Caravel reset, and power circuit
    2. Caravel power-on After FPGA bit-stream download
    3. Caravel reset released after Caravel firmware download
2. FPGA download Caravel flash content from host
3. Caravel chip initialization

Development Milestones

Caravel Tapeout Schedule （**Open: Oct, Tapeout: Dec**）

Execution plan:
https://docs.google.com/spreadsheets/d/1WV7Wh4ped0-JmsU40KdZtgDPOp3YCy2w/edit?usp=sharing&ouid=102171781329240629951&rtpof=true&sd=true

Stages of Development

Stage#1: Background Preparation (March, April)

Stage#2: Validation IP development – Caravel/FPGA (May, June)

Stage#3: FPGA Integrated Emulation (July, Aug)

Stage#4: Caravel IC Tapeout Flow & Validation Board Development (Sep - Dec)

Stage#5: Validation Test Development (Nov, Dec)

Stage#6: Silicon Validation & System online (April 2024)

Stage#1: Background Preparation (March, April)

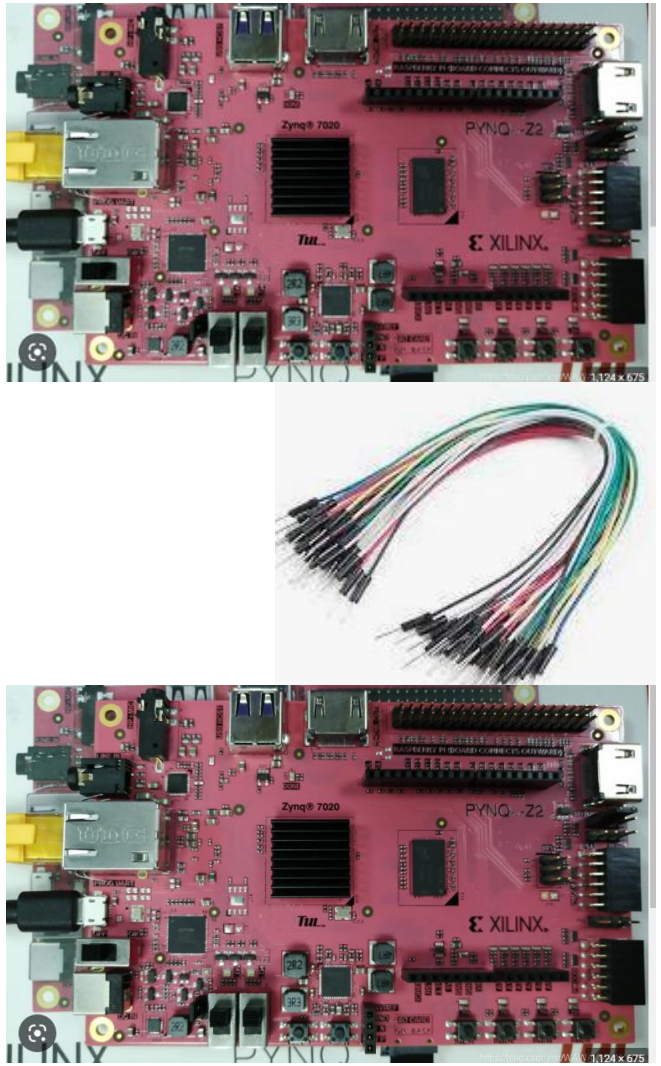
1. Tools setup - iverilog/vtag, gtkwave, Vitis, Makefile, Tcl
2. Verilog Coding - design a module (FIR)
3. FPGA-HLS
4. Caravel SOC Study
5. RISC-V Embedded Programming

Stage#2: Validation IP development (May, June)

1. Architecture & Implementation specification
2. Caravel / FPGA Validation IP Development
3. Verification software for IP & integration test
4. Caravel + FPGA Validation IP integration verification (simulation)
5. User Project Proposal for Caravel Chip tape-out

Stage#3: FPGA Integrated Emulation (July, Aug)

1. Caravel design porting to FPGA
2. Interconnect two FPGA boards
3. Software development for boot, and multiple IPs (Counter/bcd/FIR) validation
4. User Project IP development



Stage#4: Caravel IC Tape-out Flow & Validation Board Development (Sep, Oct)

ChipIglite Schedule: Submission open @Oct, Close @December

1. Caravel IC backend flow
2. Efabless project application
3. Validation board design

Stage#5: Validation Test Development & System online (Nov, Dec)

1. Validation Test Development
2. Board manufacturing and bring-up (see if we can get an existing Caravel chip)
3. Validation Platform goes online open for user project development

Project Execution Logistics

Project Execution Logistics

- Google Meet Notice with zoom meeting – issued by boledulab
  - Zoom meeting linked with Youtube live
- Teams - fsic (all), fsic-carvel-ip, fsic-fpga-ip, fsic-carvel, fsic-fpga, fsic-sw, fsic-system
  - Team modulator
  - Each member can participate two teams (major/minor)
- Discussion in Discord Channel (全端 ic 設計工程師開發流程)
  - https://discordapp.com/channels/838422912507052062/1077220224820068363
- Execution Plan
  - https://docs.google.com/spreadsheets/d/1WV7Wh4ped0-JmsU40KdZtgDPOp3YCy2w/edit#gid=392734974
  - Milestones, meeting minutes, action items, team status
- Development Database – boledu Github https://github.com/bol-edu
  - Mirror to Accomdemy Github

工作項目及分組

1. caravel-ip: Caravel SOC 驗證平台 IP 設計 （ Verilog / HLS-C++)
2. fpga-ip: FPGA 驗證平台 IP 設計（ Verilog / HLS-C++) -fsic-fpga-ip
3. fpga: 整合 FPGA 模擬平台開發
4. caravel： Caravel SOC (Efabless / TSMC) 設計整合，驗證，後端，下線
5. sw: 驗證韌體（Firmware）及測試軟體開發
6. system: 系統設計 – FPGA Board Interconnect, IC 包裝, PCB 設計

Modulators

姓名（中文/英文）	
劉家豪	fsic-fpga-ip
郭瑞申/Ray	fsic-caravel
FranceChu	fsic-sw
陳耀宗/Ralph	fsic-fpga
林奕杰	fsic-fpga-ip
撒景賢	fsic-system
蕭良宇/liangyu	fsic-sw
魏選賢	fsic-caravel-ip
Patrick Lin	fsic-fpga
張瑋鑫	fsic-caravel-ip

Meeting Minutes

Date	Minutes	Action items	AR Team
00-00-00	Template: <Status> : what is done in this week, issues <Decision>: decision made for an issue <Ref> : reference link on ppt, work, ... latest date in front	Template: <team>: Todo item	

Meeting Agenda - Hosted by Modulator

- Action item review from last meeting
- Next Actions - practice/lab/design activity
- Presentation & Discussion

Meeting Time: Each Monday @8pm

Key Milestones & Celebration/Award (Contributor only)

1. FPGA Integration and Demo in COSCUP (7/29, 7/30)
   https://coscup.org/2023/en/landing?gclid=CjwKCAiAjPyfBhBMEiwAB2CCIlYShEsWaQaYxy61S6bvSSHWcK68QFwxrQ63AZowcYbn5UJ76MwAFRoCM8AQAvD_BwE

2. ChipIglite Submission (Tapeout) in Oct – Dec

chipIgnite Shuttle Schedule

	2209C	2211Q	2304C	2306Q
Engineer Samples	300 WCSP	100 QFN	300 WCSP	100 QFN
Evaluation Boards	5	5	5	5
Tapeout Date	September 19, 2022	November 14, 2022	April 3, 2023	June 12, 2023
Delivery Date	February 7, 2023	March 9, 2023	July 27, 2023	October 5, 2023

3. FSIC chip successfully runs on Validation Platform (est: April 2024)

Let’s Start Working - First week

- Verilog Tool (iverilog, gtkwave, vtags) setup
- Caravel Simulation Environment setup

- Caravel SoC 專案手冊: (Kevin)
  - https://github.com/bol-edu/caravel-soc/files/10857546/caravel-soc_project-manual.pdf