Effective Power/Ground Plane Decoupling for PCB

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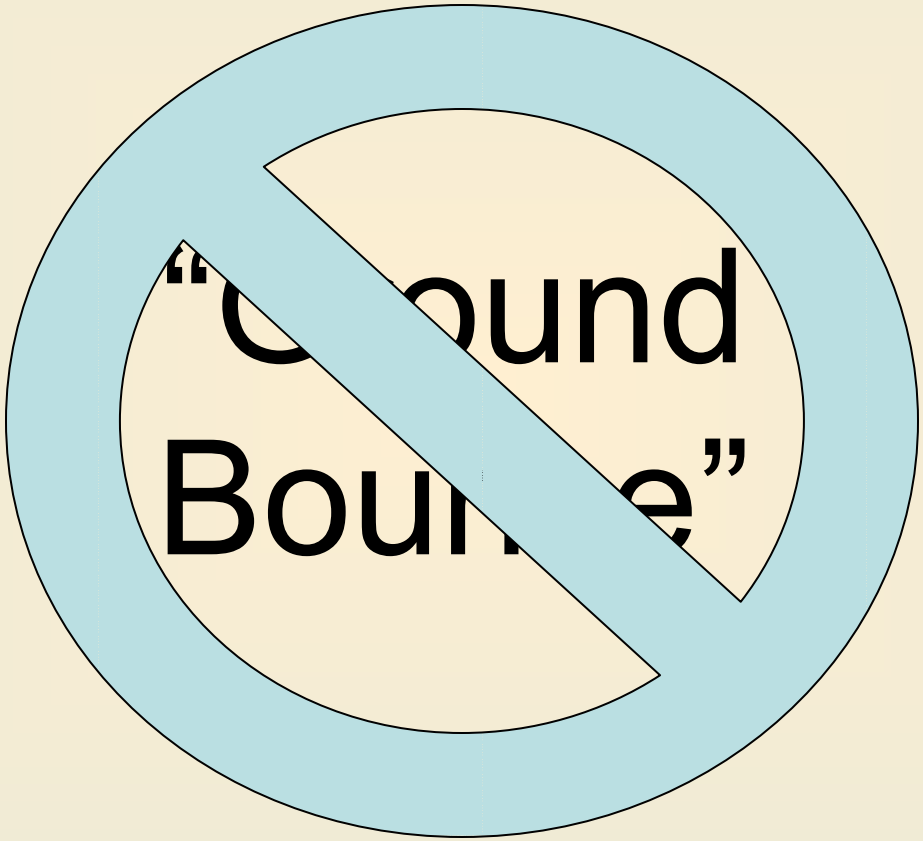
Power Plane Noise Control



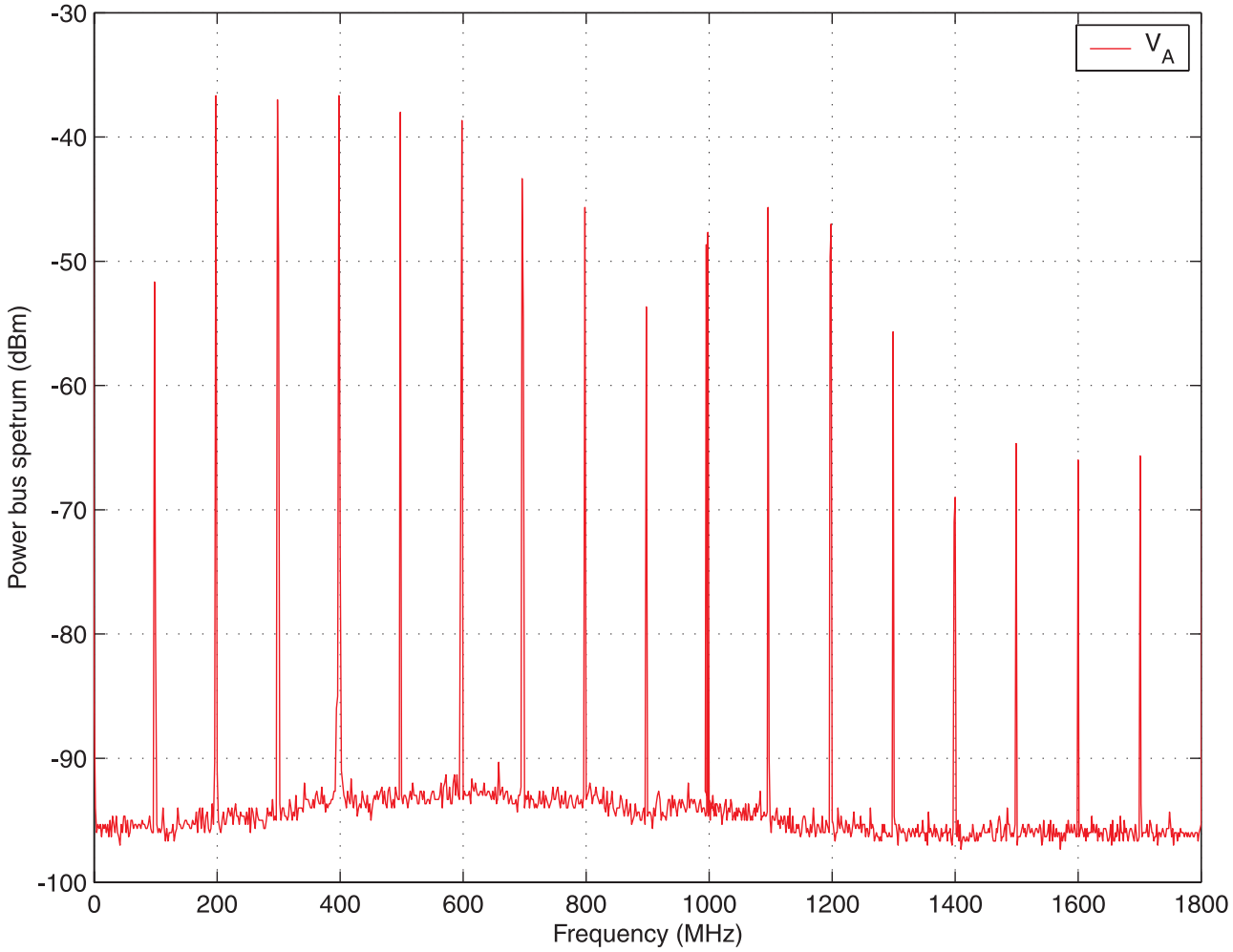
Power/Ground-Reference Plane Noise

- Must consider TWO Major Factors
  - EMC -- Reduce noise along edge of board from IC somewhere else
  - Functionality -- Provide IC with sufficient charge
- Decoupling strategies are FULL of ***Myths***
  - Consider the physics
  - Don't forget ***Inductance!***

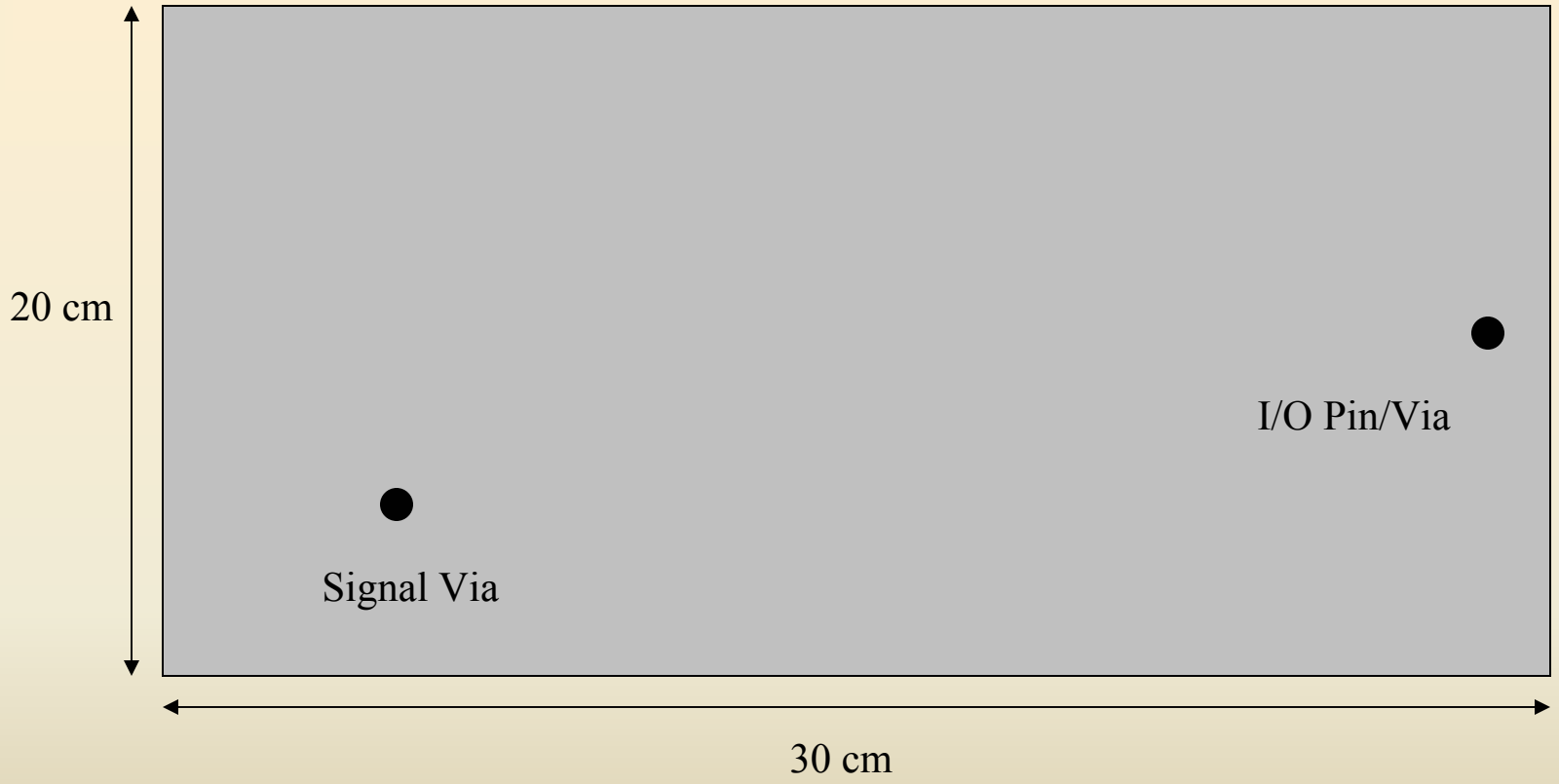
Source of Power/Ground-Reference Plane Noise

- Power requirements from IC during switching
- Critical Net currents routed through via

Power Bus Spectrum
Clock Driver IDT74FCT807

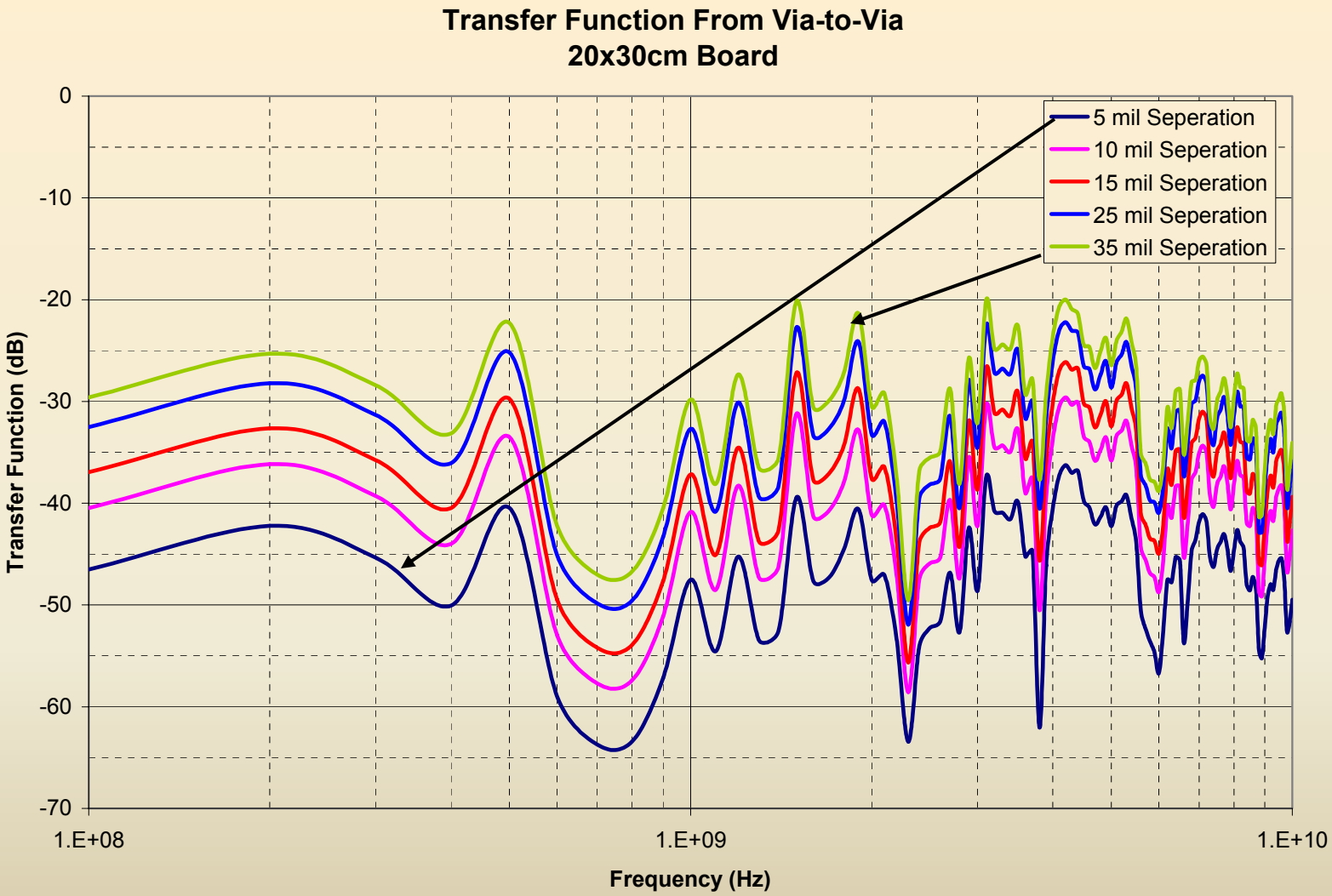


Noise Injected between Planes Due to Critical Net Through Via



FR4 ε_r=4.2 Loss tan=0.02

Transfer Function from Via to I/O Pin



Decoupling Must be Analyzed in Different Ways for Different Functions

- EMC
  - Resonance big concern
  - Requires STEADY-STATE analysis
    - Frequency Domain
  - Transfer function analysis
    - Eliminate noise along edge of board due to ASIC/IC located far away

Decoupling Must be Analyzed in Different Ways for Different Functions

- Provide Charge to ASIC/IC
  - Requires TRANSIENT analysis
  - Charge will NOT travel from far corners of the board fast enough
  - Local decoupling capacitors dominate
  - Impedance at ASIC/IC pins important

Steady-State Analysis

- Measurements and Simulations
- Test Board with Decoupling capacitors every 1” square

Test Board Ports

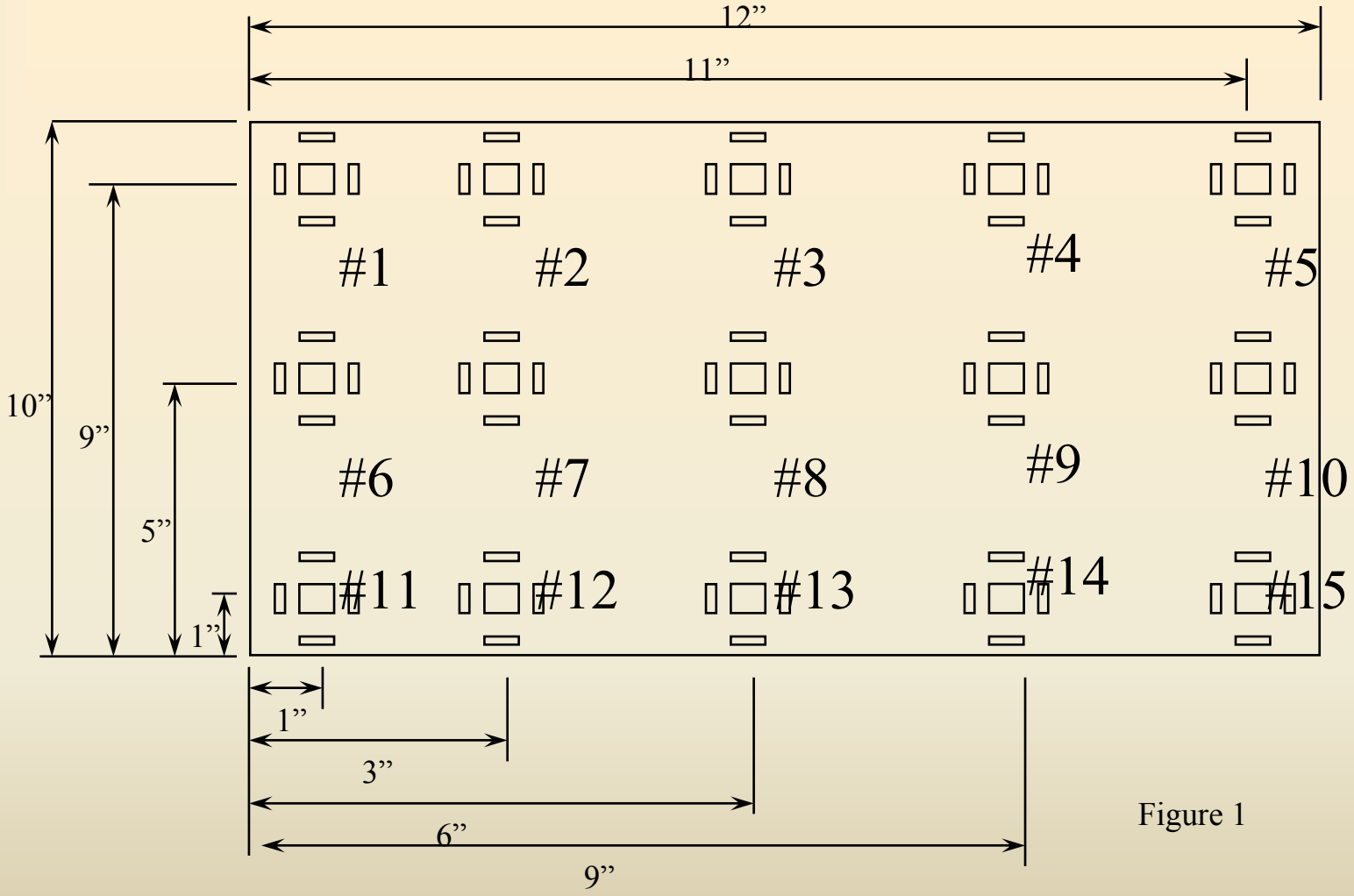
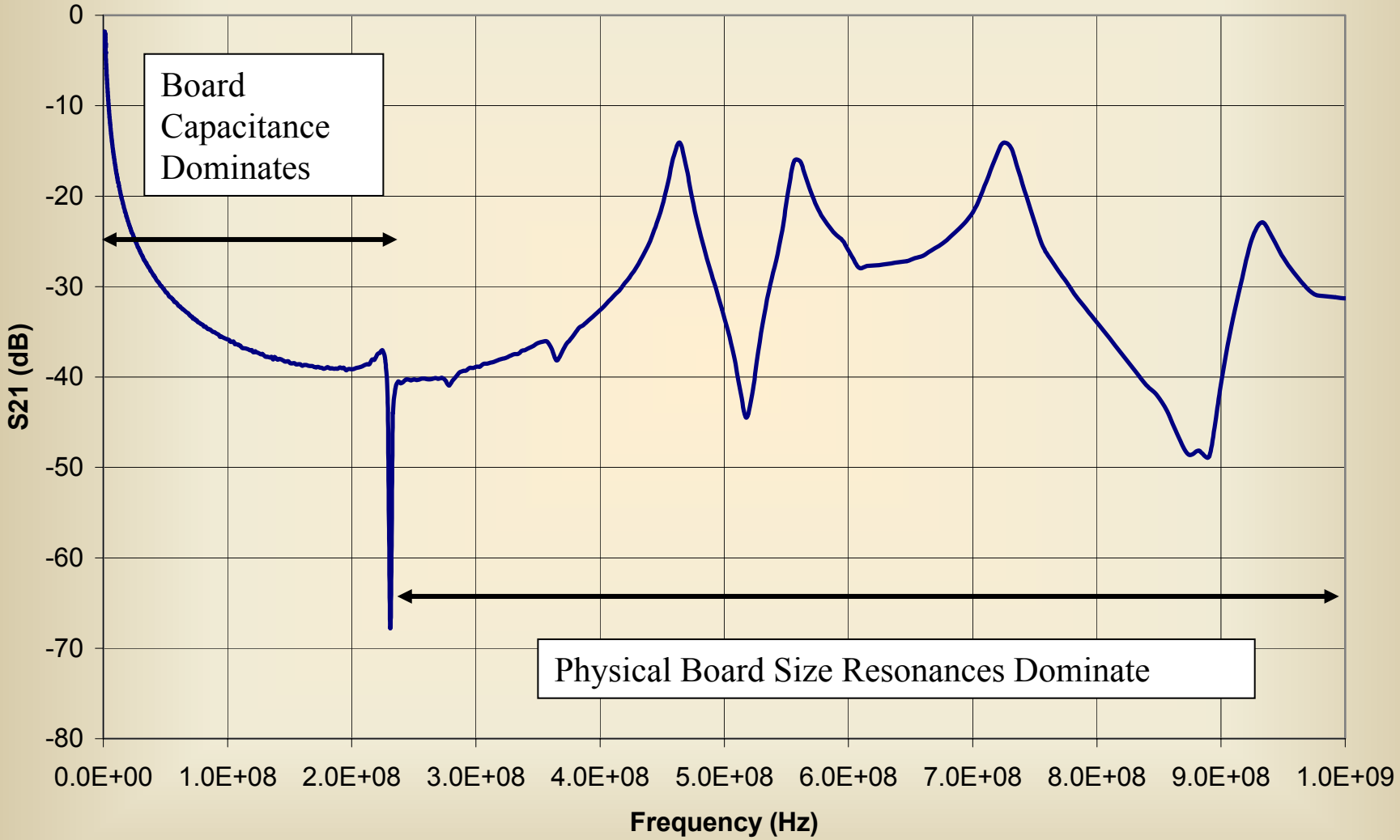


Figure 1

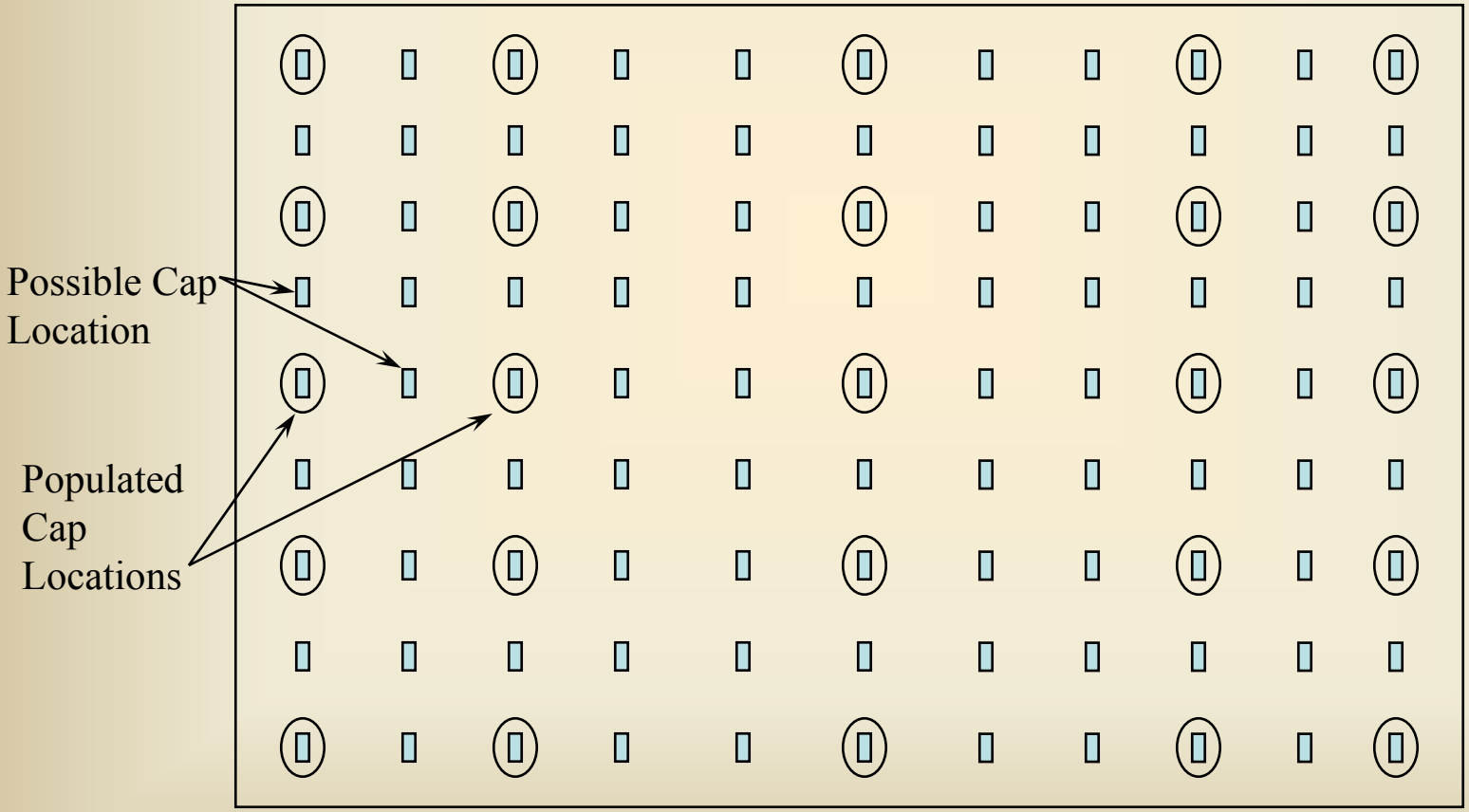
S21 Used for Decoupling “Goodness”

- Ratio of Power ‘out’ to power ‘in’
- Better Indicator of EMI noise transmission across board
- Also used to validate simulations

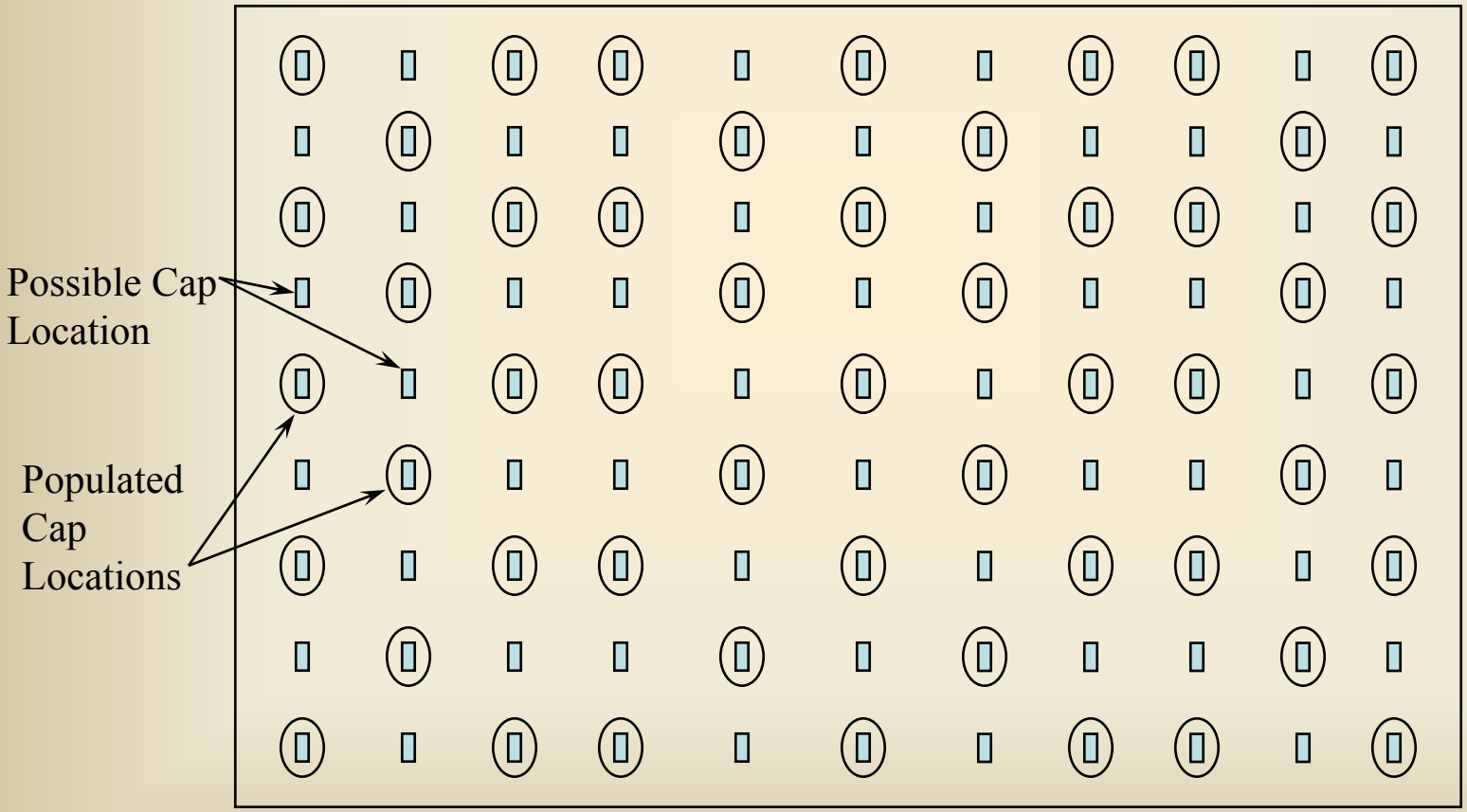
Measured S21 for 12" x 10" PC Board Between Power/Ground Planes with No Decoupling Capacitors (Measured Center to Corner)



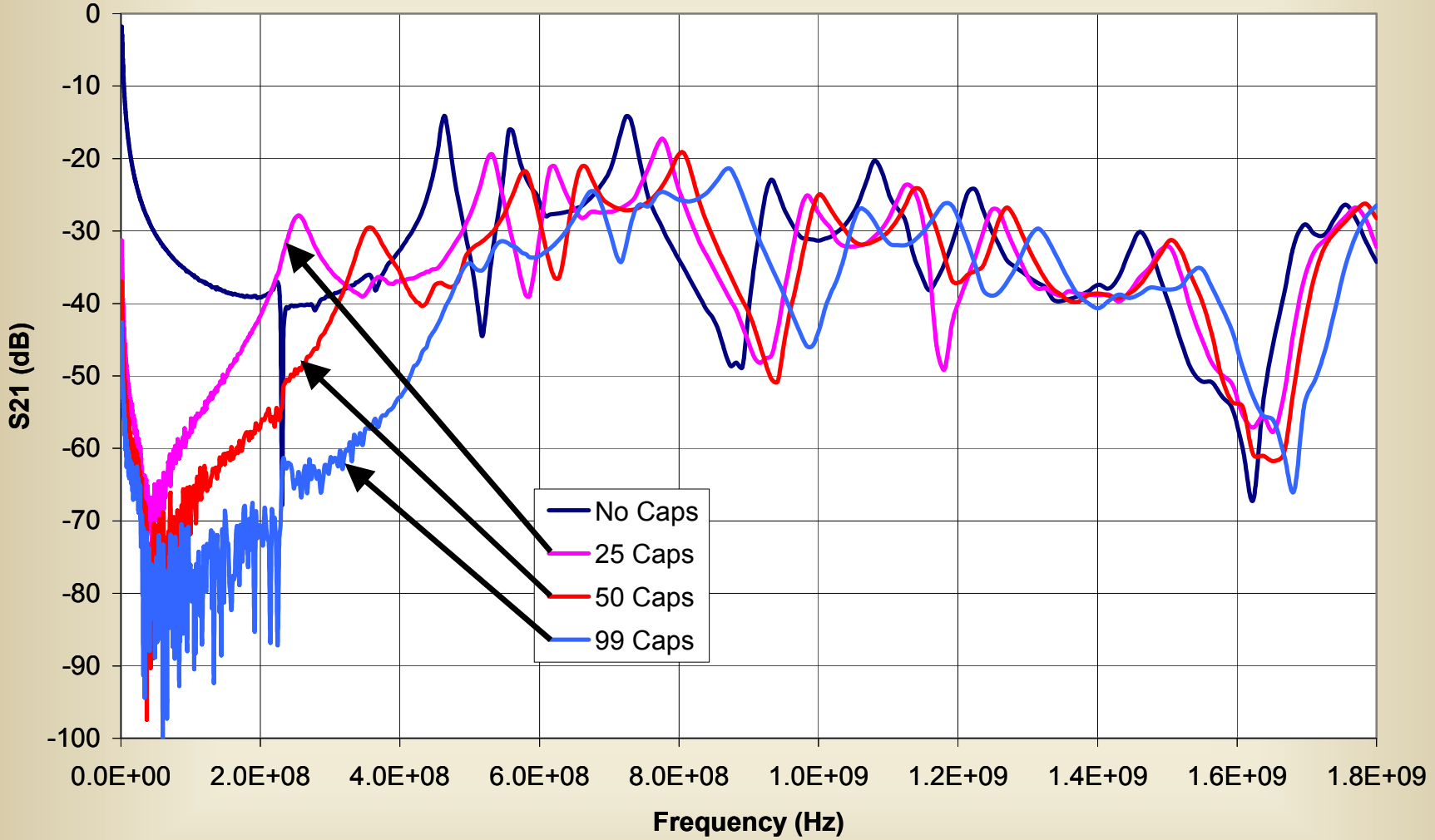
Test Board Decoupling Capacitor Placement for 25 .01 uf Caps



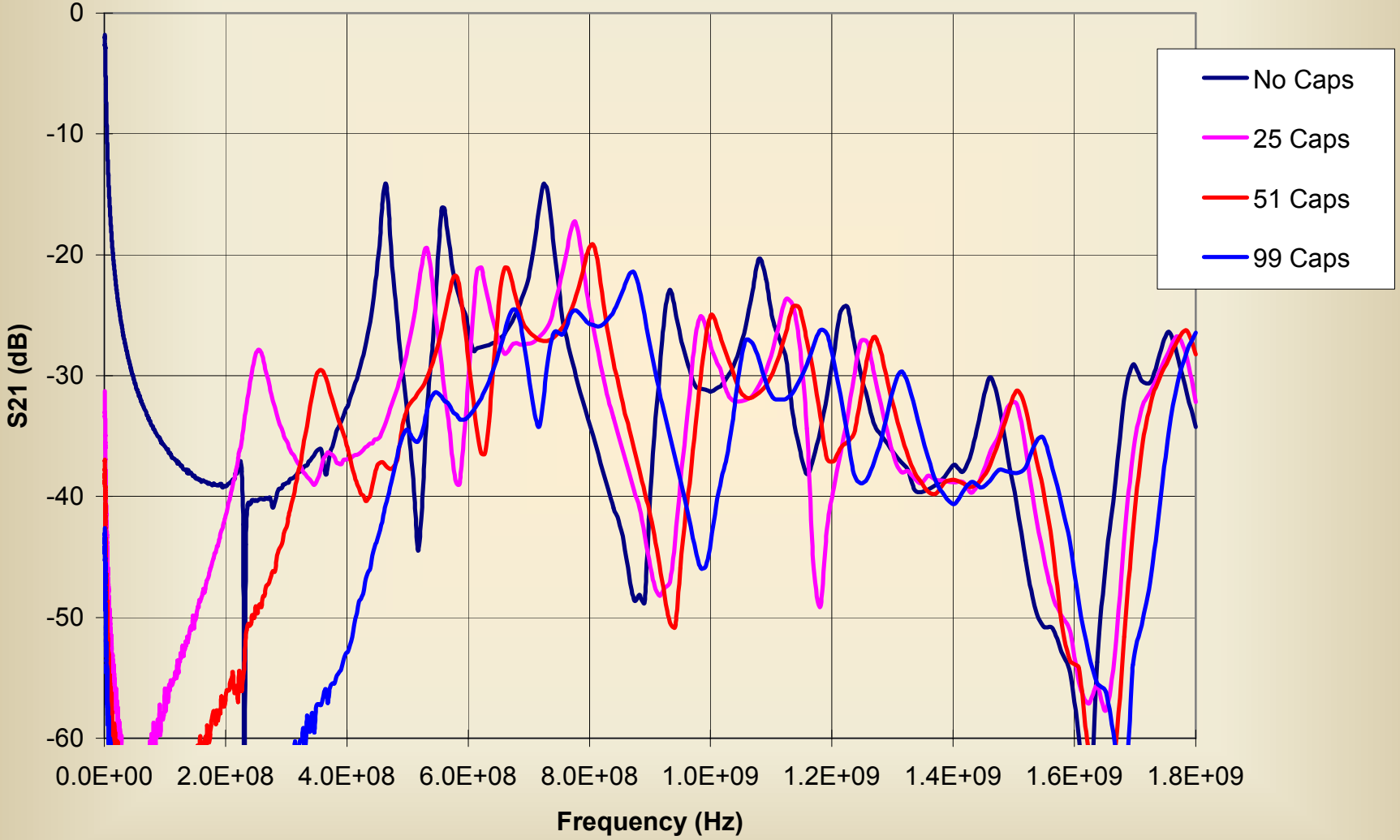
Test Board Decoupling Capacitor Placement for 51 .01 uf Caps



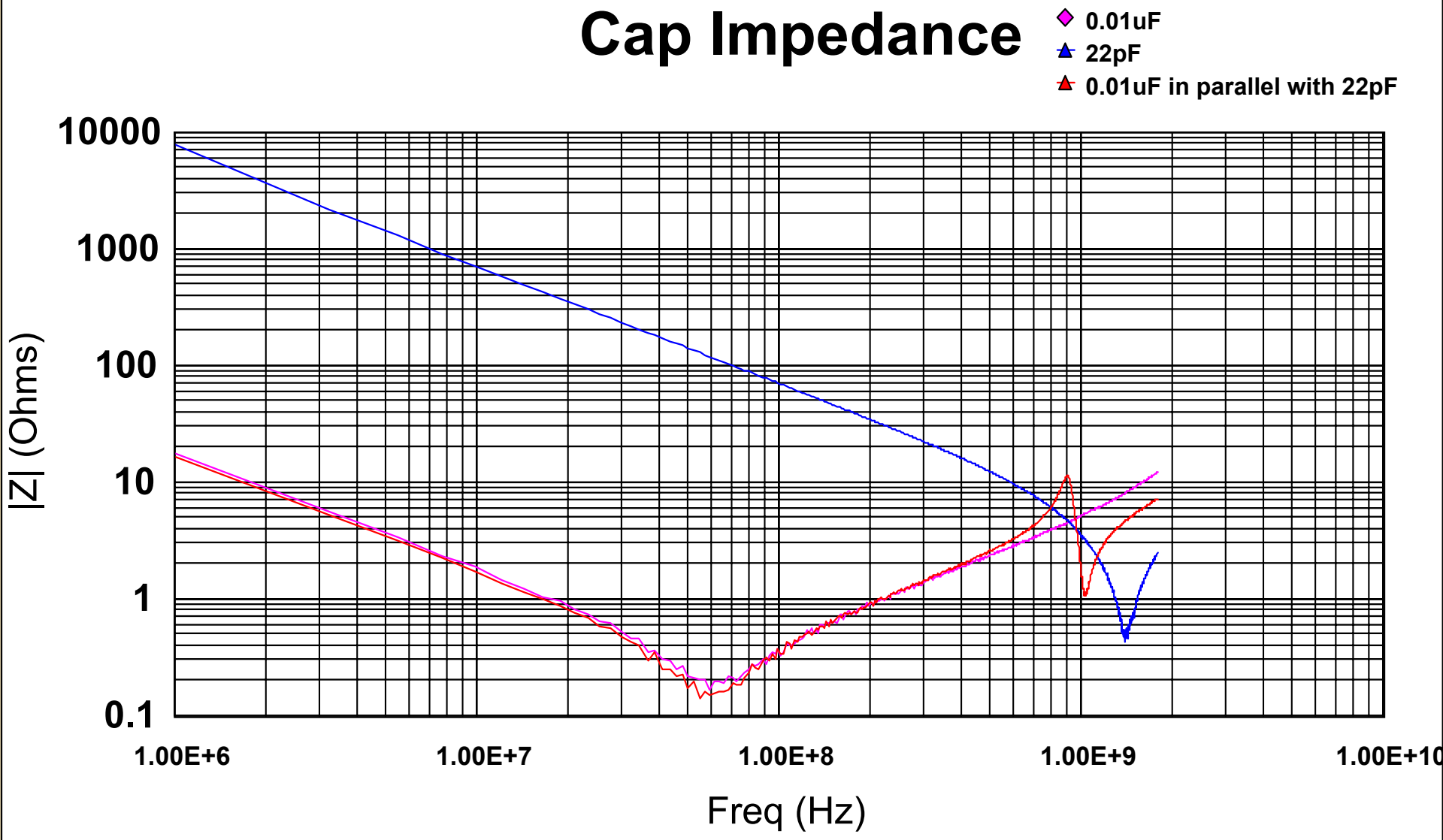
Measured S21 for 12" x 10" PC Board Between Power/Ground Planes with Various Amounts of Decoupling Capacitors (Measured Center to Corner)



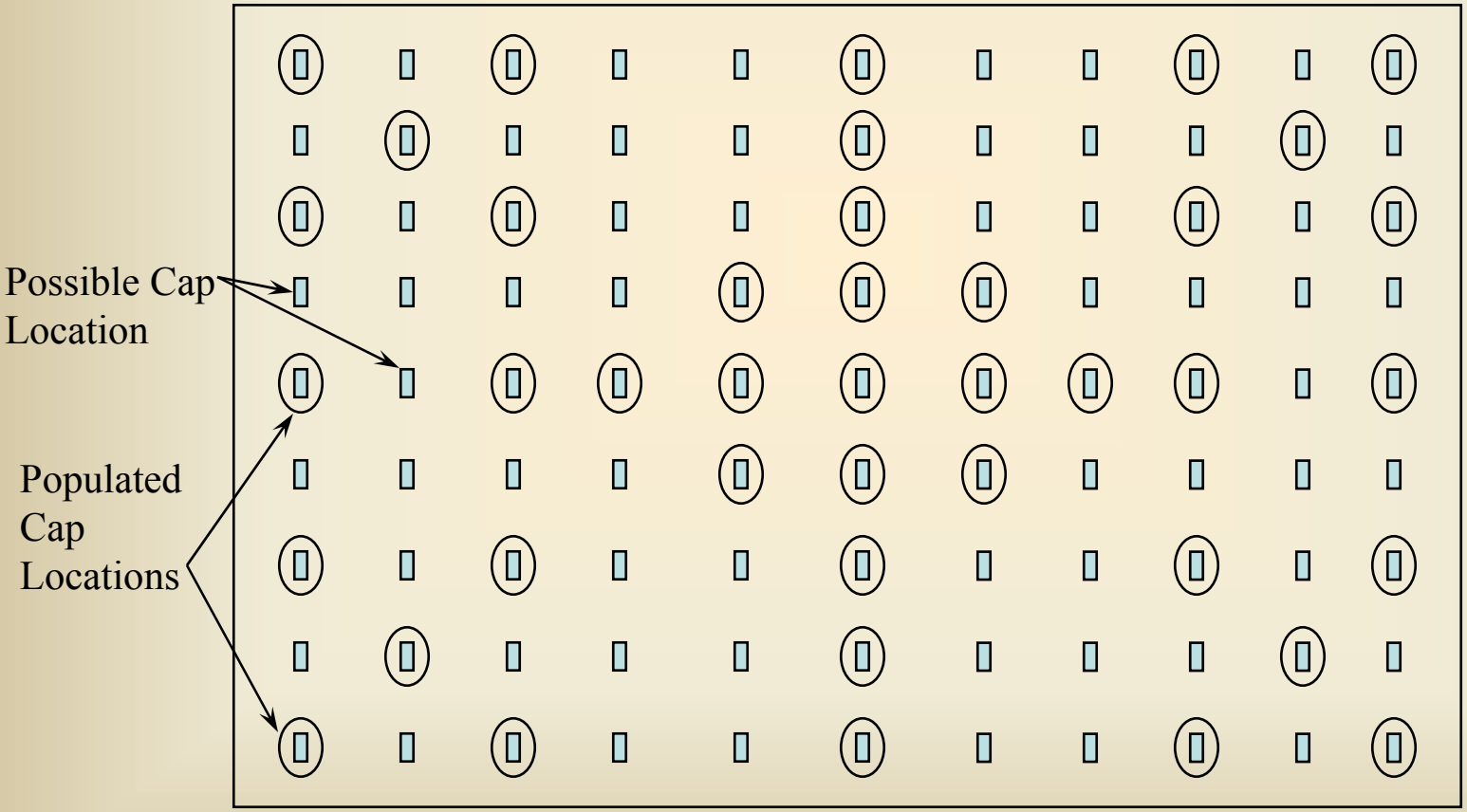
S21 Between Port #8 and Port #1 on Test Board
With Various Amounts of .01 uf Decoupling Capacitors



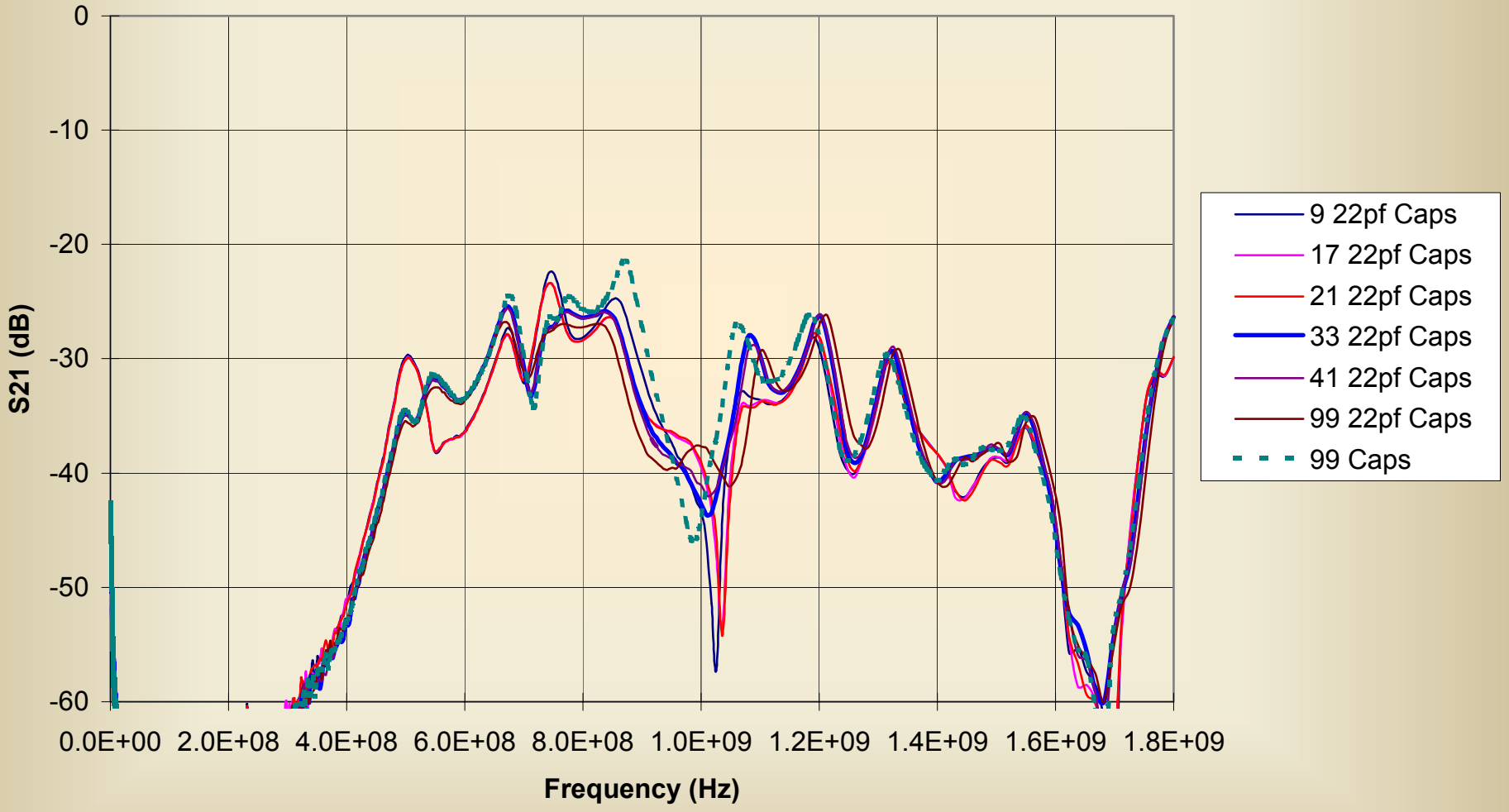
Cap Impedance



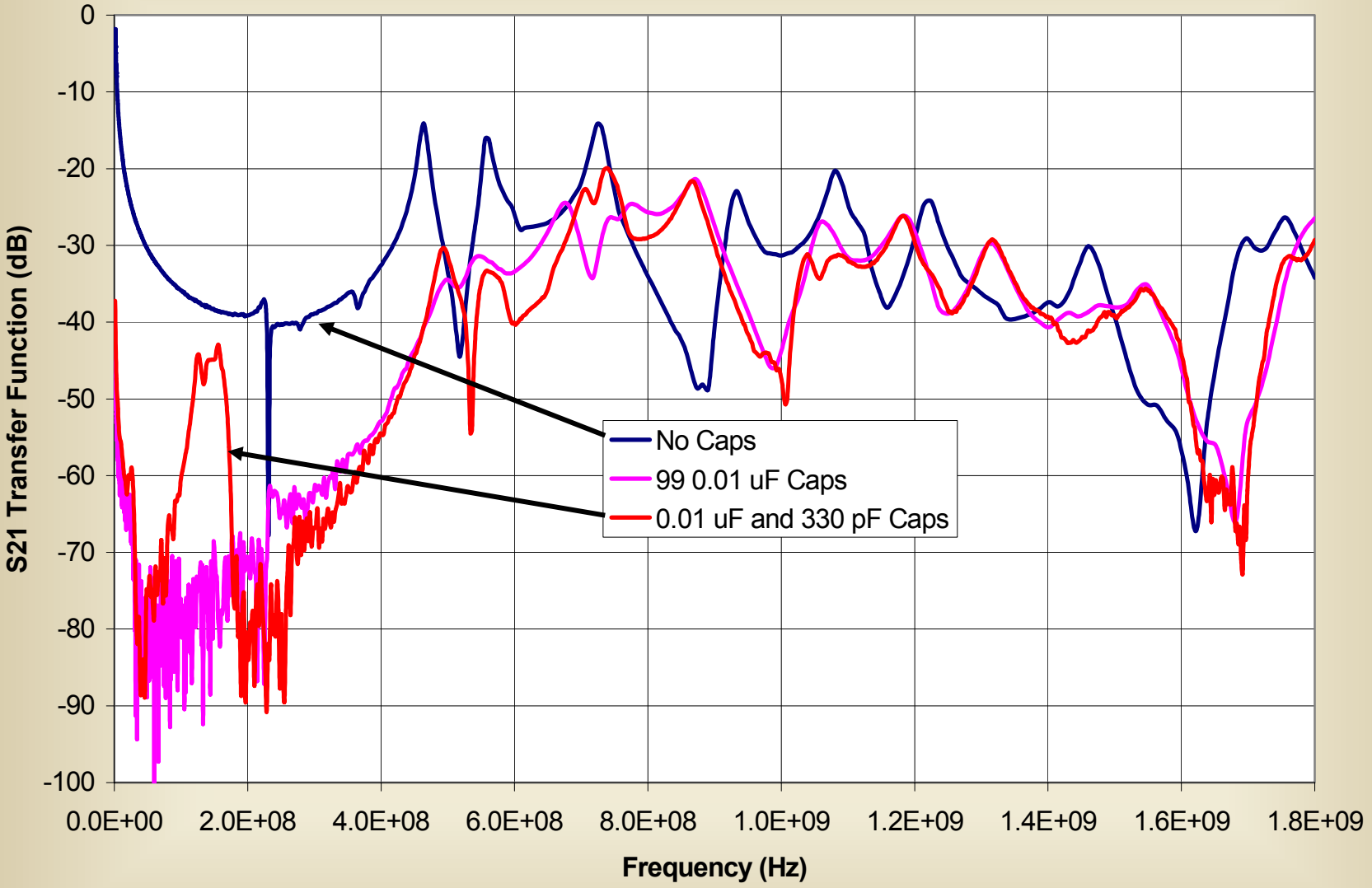
Test Board Decoupling Capacitor Placement for 41 22pf Caps (In Addition to 99 .01uf Caps)

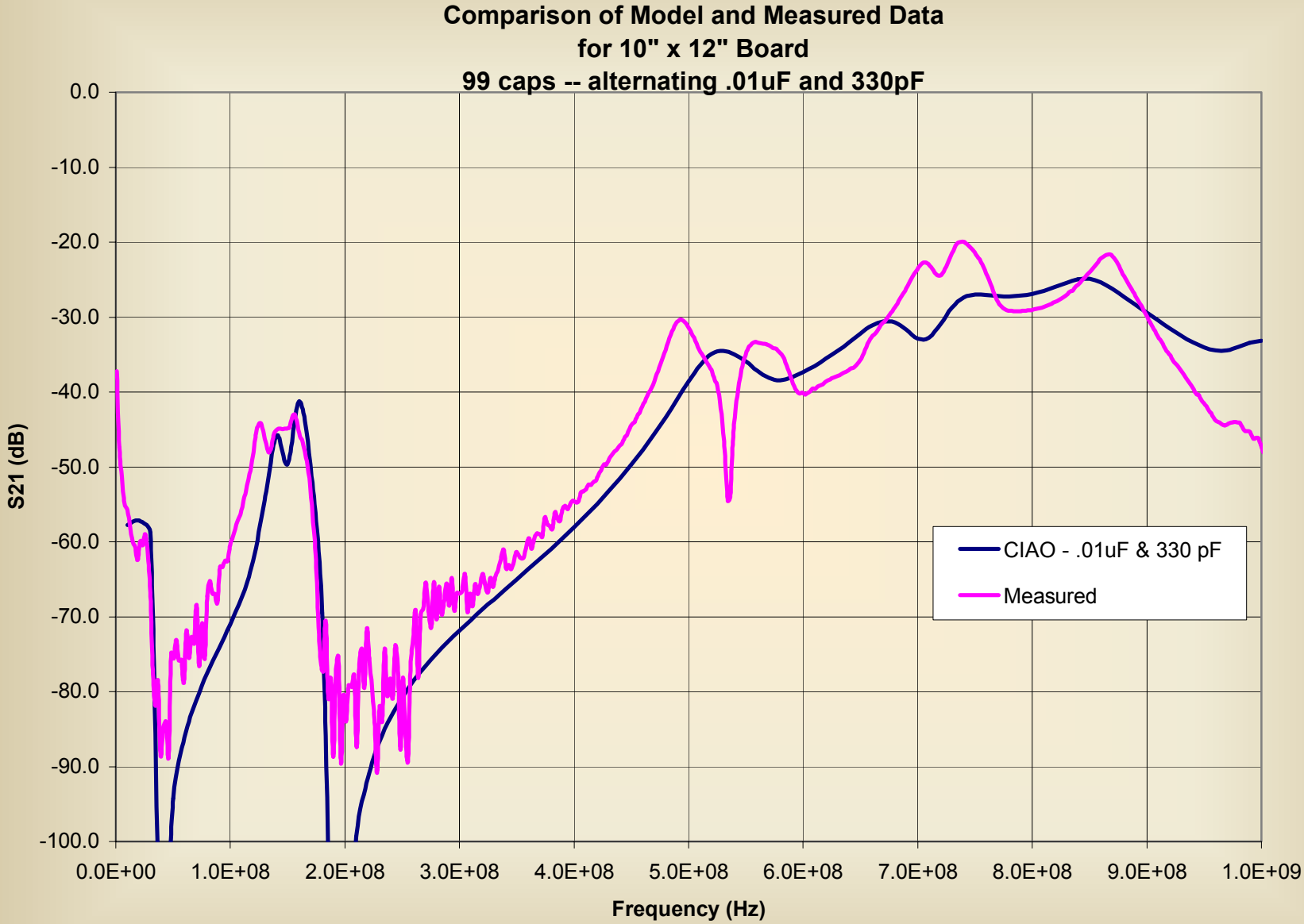


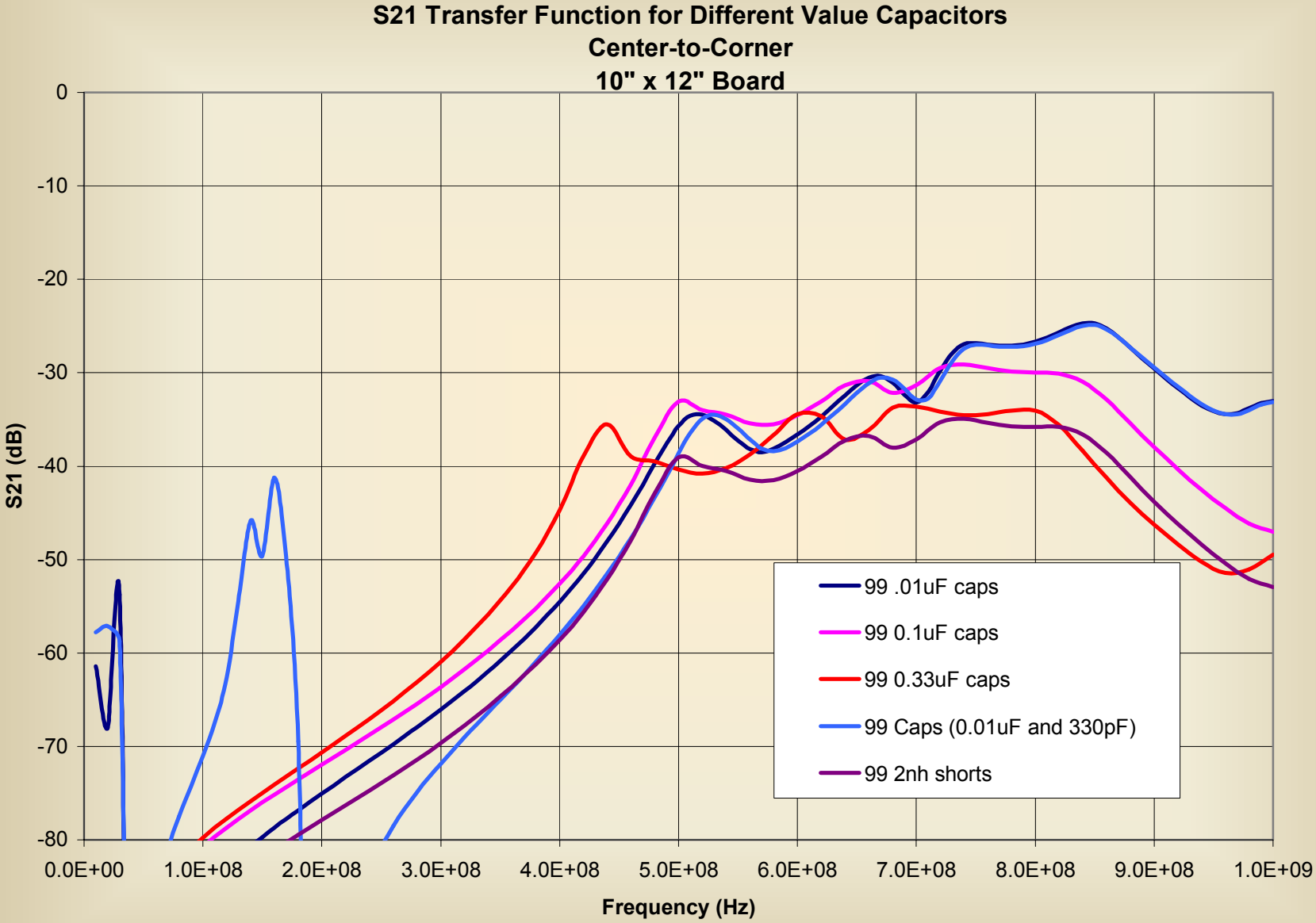
S21 Between Port #8 and Port #1 on Test Board With 99 .01 uf Decoupling Capacitors and Various Amounts of 22pf Capacitors Added



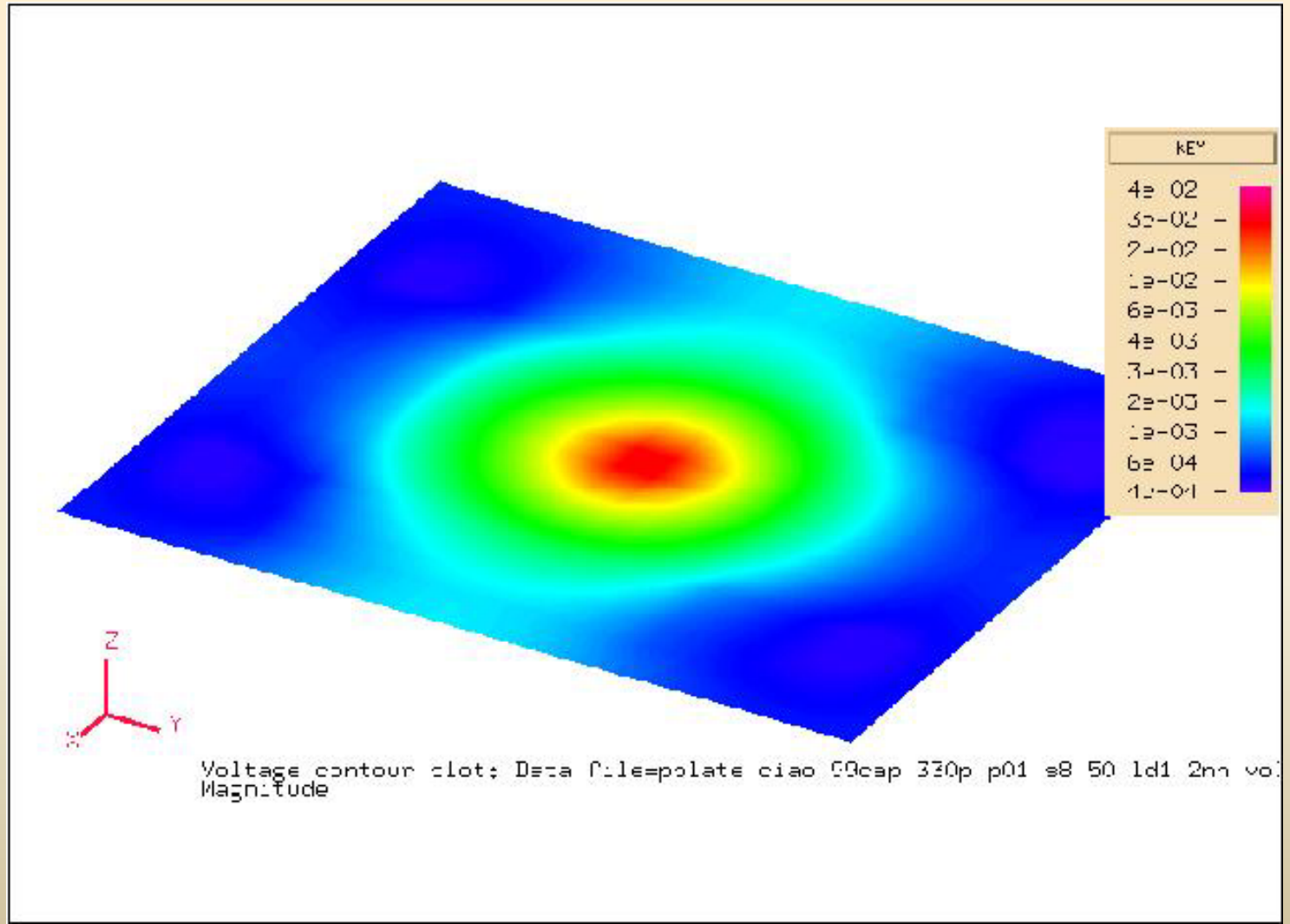
Measured Comparison of Multiple and Single Value Decoupling Capacitor Strategies



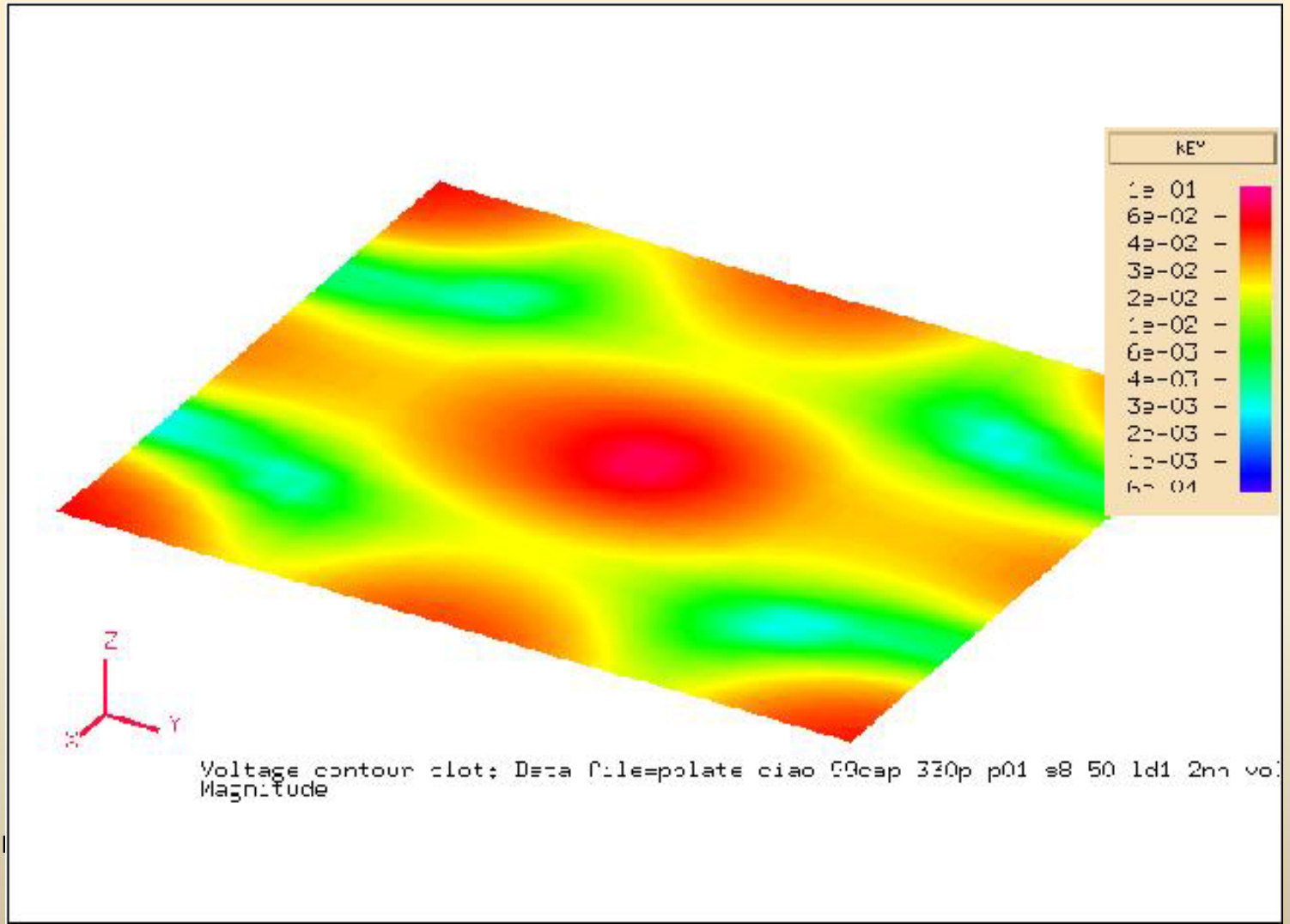

Comparison of Model and Measured Data
for 10" x 12" Board
99 caps -- alternating .01uF and 330pF
S21 (dB)
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
0.0E+00
1.0E+08
2.0E+08
3.0E+08
4.0E+08
5.0E+08
6.0E+08
7.0E+08
8.0E+08
9.0E+08
1.0E+09
Frequency (Hz)
CIAO - .01uF & 330 pF
Measured


S21 Transfer Function for Different Value Capacitors
Center-to-Corner
10" x 12" Board
S21 (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
0.0E+00
1.0E+08
2.0E+08
3.0E+08
4.0E+08
5.0E+08
6.0E+08
7.0E+08
8.0E+08
9.0E+08
1.0E+09
Frequency (Hz)
99 .01uF caps
99 0.1uF caps
99 0.33uF caps
99 Caps (0.01uF and 330pF)
99 2nh shorts

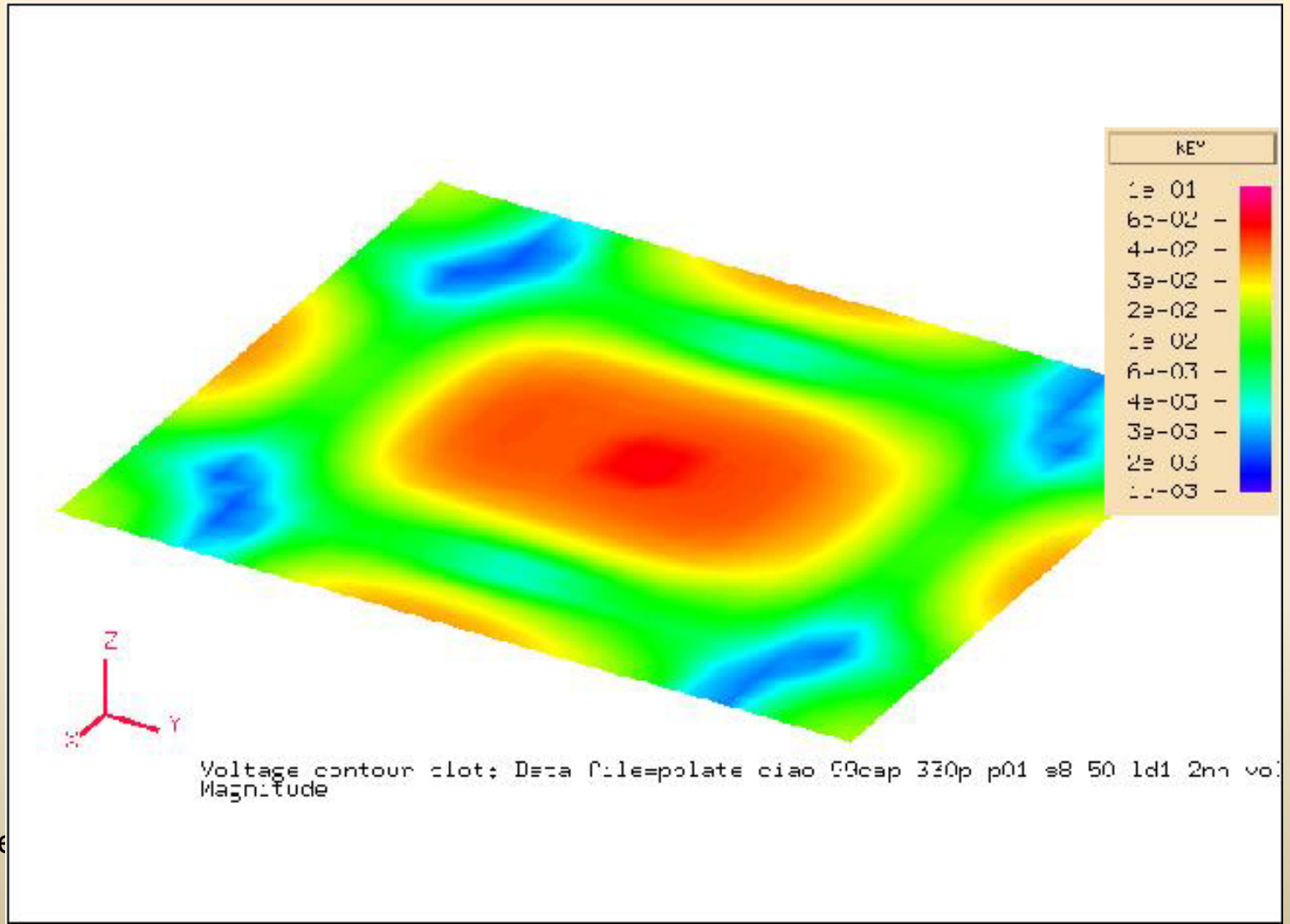
Voltage Distribution @ 350 MHz .01uF and 330pF Case (Source in Center)



Voltage Distribution @ 750 MHz .01uF and 330pF Case (Source in Center)

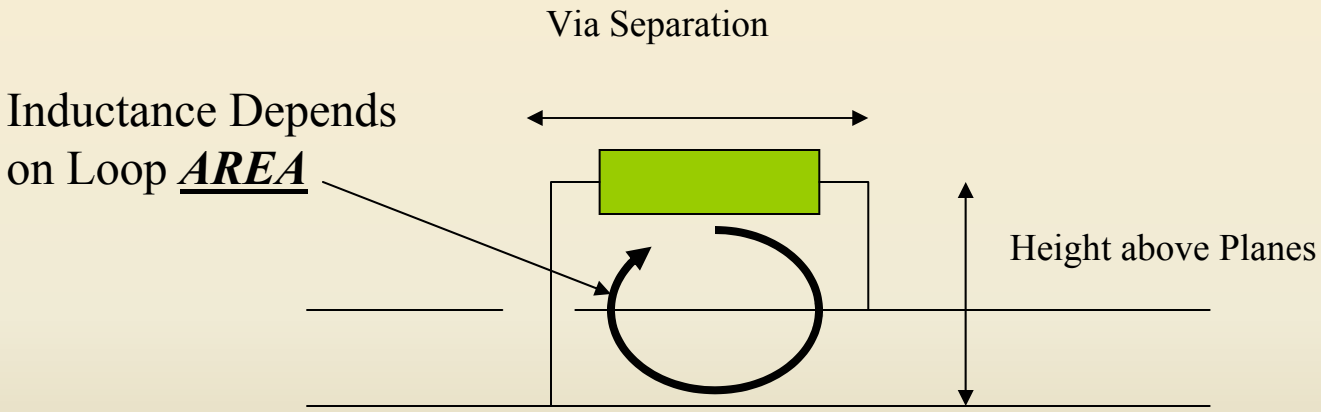


Voltage Distribution @ 950 MHz .01uF and 330pF Case (Source in Center)



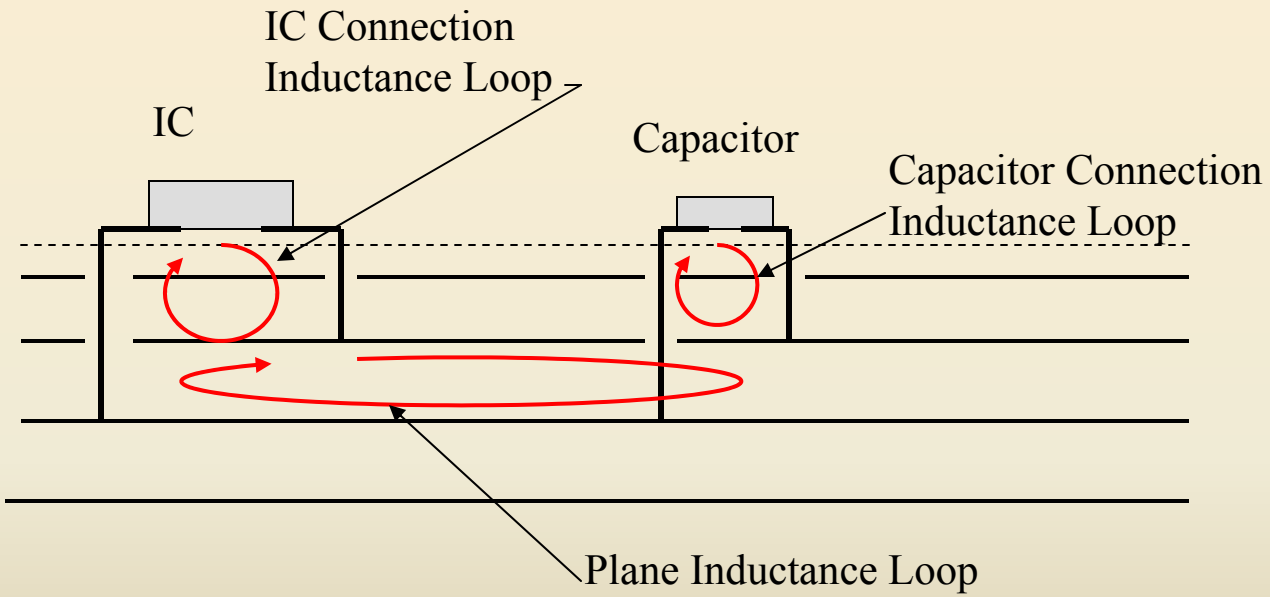
Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible

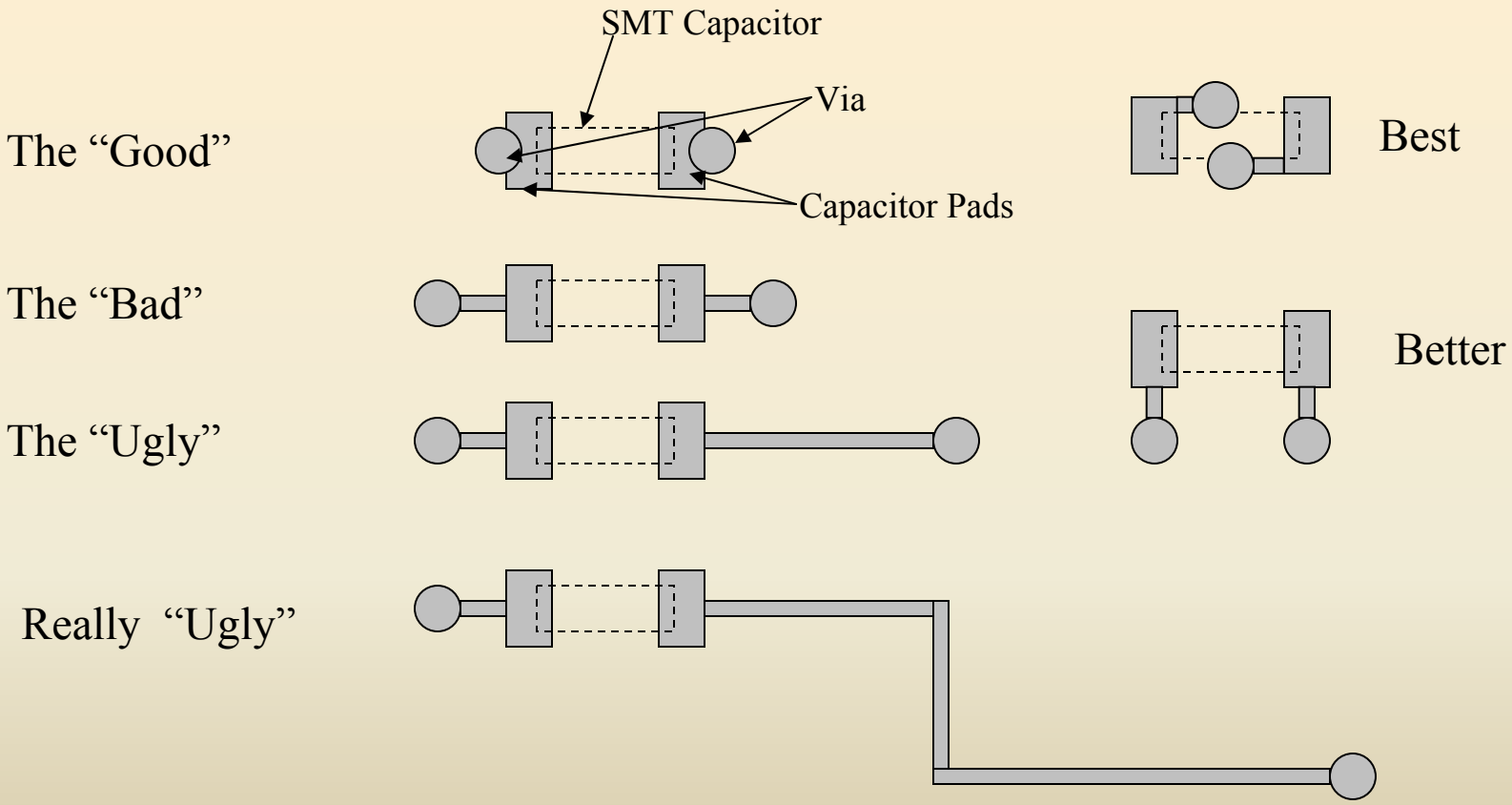


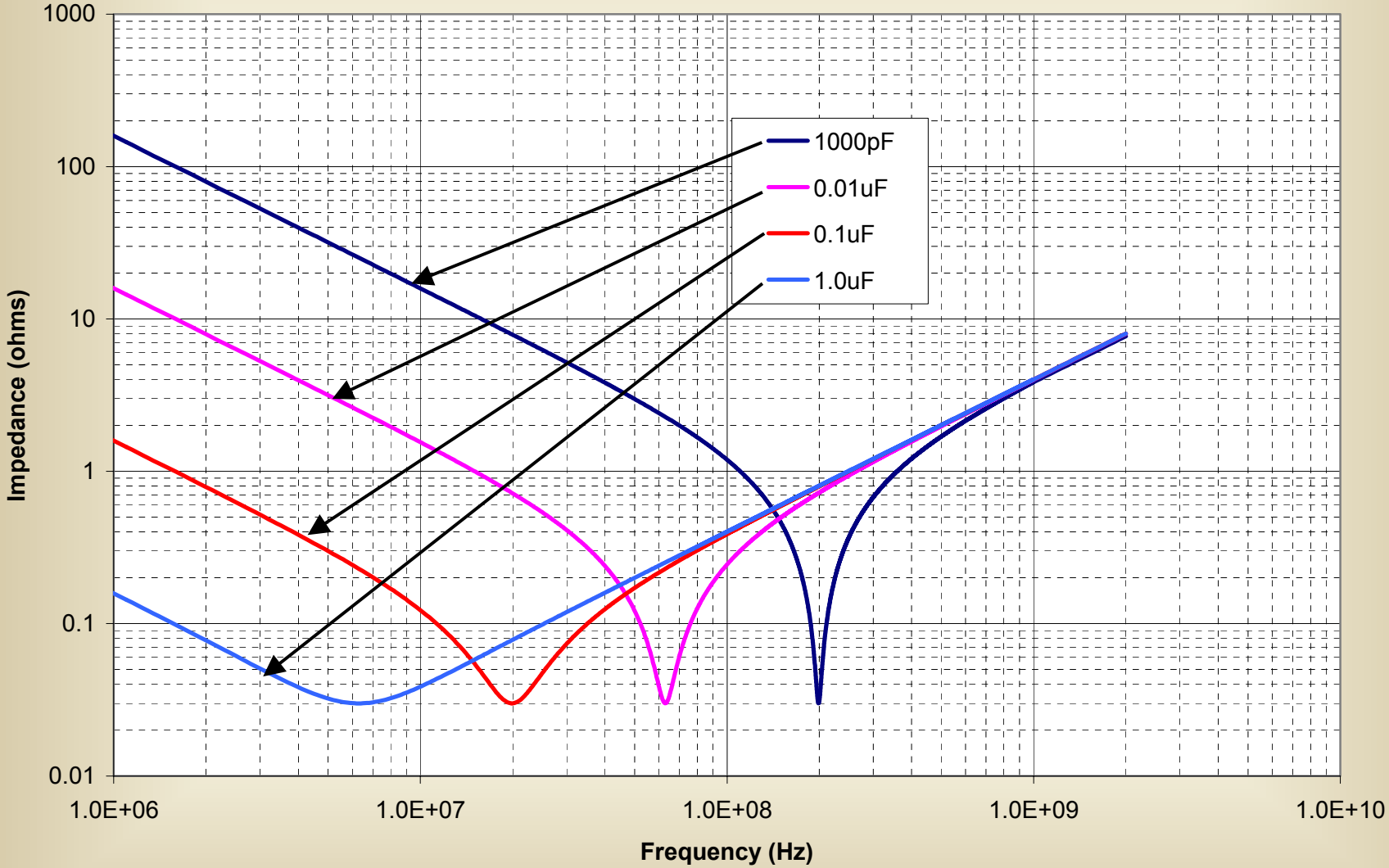
Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible



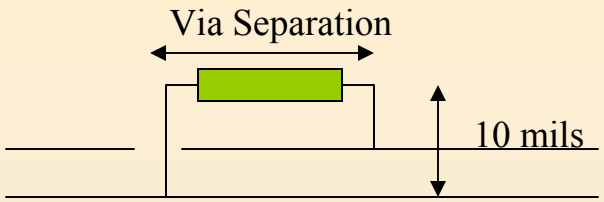
Via Configuration Can Change Inductance




Comparison of Decoupling Capacitor Impedance
100 mil Between Vias & 10 mil to Planes
1000
100
10
1
0.1
0.01
Impedance (ohms)
1000pF
0.01uF
0.1uF
1.0uF
1.0E+06
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)

Comparison of Decoupling Capacitor Via Separation Distance Effects

0.1 uF Capacitor



Via Seperation (mils)	Inductance (nH)	Impedance @ 1 GHz (ohms)
20	.06	.41
40	0.21	1.3
60	0.36	2.33
80	0.5	3.1
100	0.64	4.0
150	1.0	6.23
200	1.4	8.5
300	2.1	12.69
400	2.75	17.3
500	3.5	21.7

Example Connection Inductance Values

Spacing between Vias	Complex Formula (20 mils to plane)	Simple rect loop (20 mils to plane)	Complex Formula (10 mils to plane)	Simple rect loop (10 mils to plane)
0805 + 2*10mil	3.0 nH	3.1 nH	2 nH	1.38 nH
0805 + 2*100mil	4.1 nH	4.3 nH	3 nH	2.0 nH
0805 + 2*160mil	5.1 nH	5.1 nH	3.5 nH	2.5 nH
0603 + 2*10mil	2.3 nH	1.74 nH	1.1 nH	0.8 nH
0603 + 2*100mil	3.3 nH	3.15 nH	2.1 nH	1.5 nH
0603 + 2*160mil	4.2 nH	4.3 nH	2.4 nH	2.07 nH

Sources for complex formula:

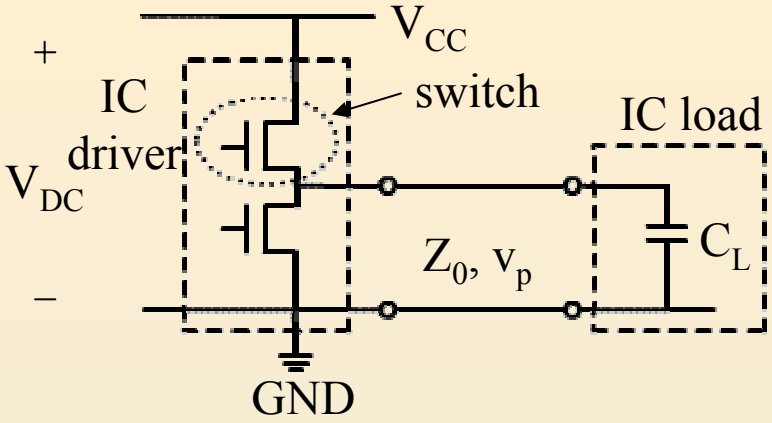
Knighten, James L., Bruce Archambeault, Jun Fan, Samuel Connor, James L. Drewniak, "PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?," *IEEE EMC Society Newsletter*, Issue No. x, Winter 2006, pp. 56-67. (www.emcs.org)

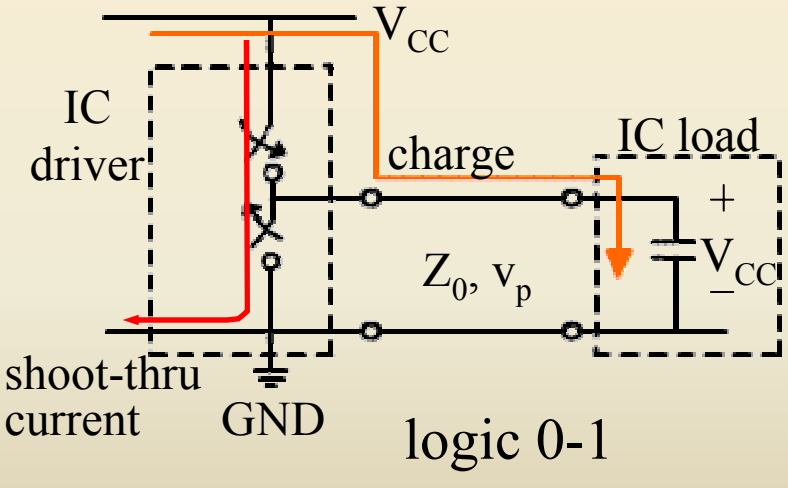
Fan, Jun, Wei Cui, James L. Drewniak, Thomas Van Doren, and James L. Knighten, "Estimating the Noise Mitigating Effect of Local Decoupling in Printed Circuit Boards," *IEEE Trans. on Advanced Packaging*, Vol. 25, No. 2, May 2002, pp. 154-165.

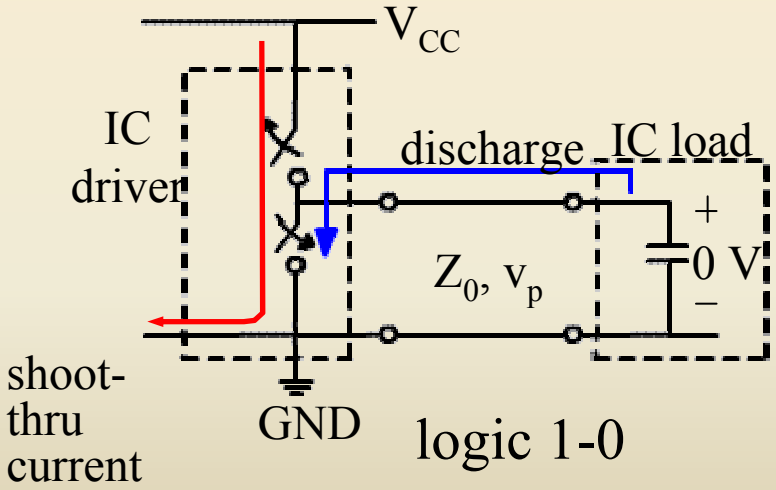
Transient Analysis
(Time Limited)

- Provide charge to ASIC/IC
- Inductance dominates impedance
  - Loop area 1st order effect
- Traditional analysis not accurate enough

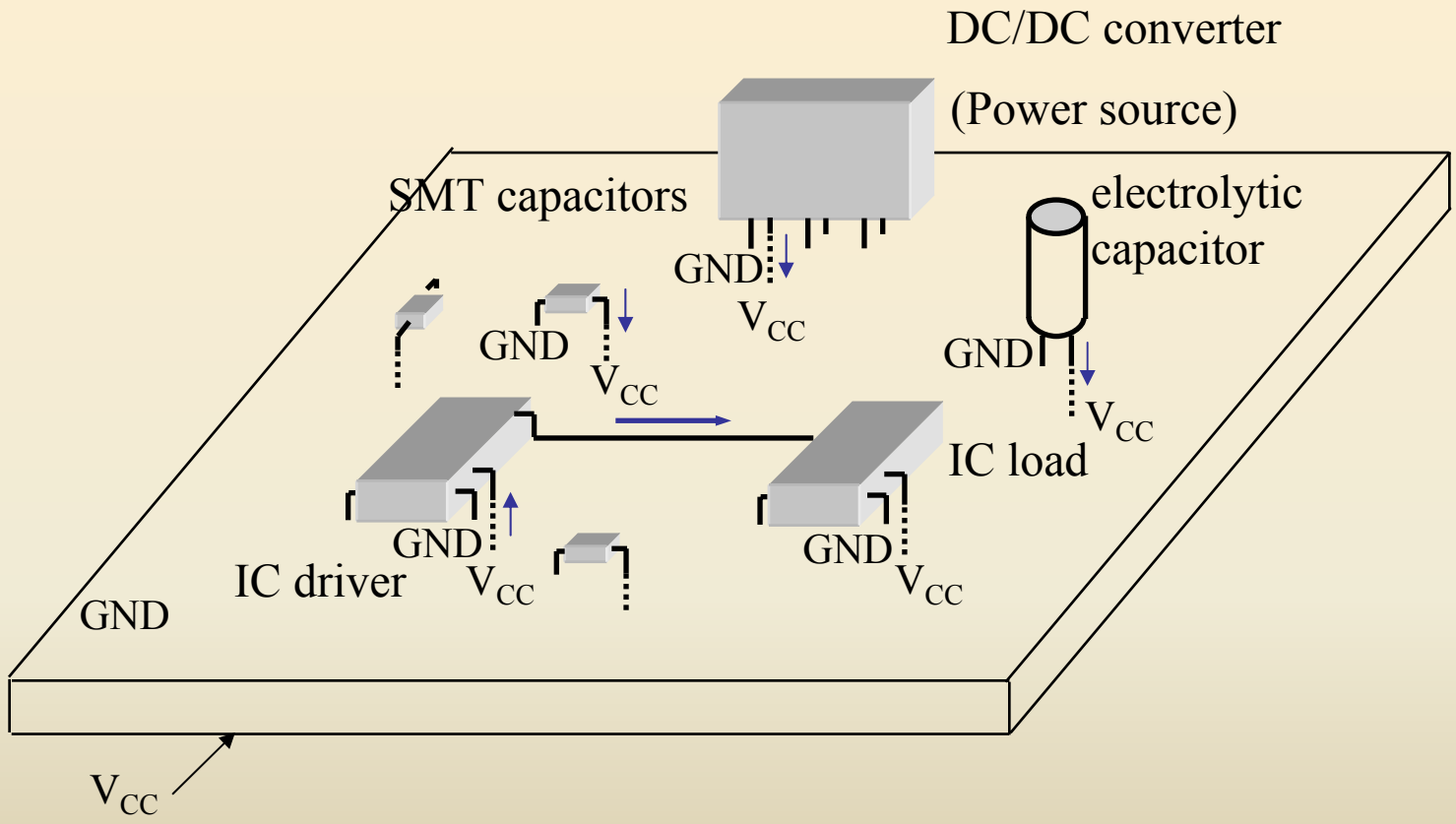
Current in IC During Logic Transitions (CMOS)



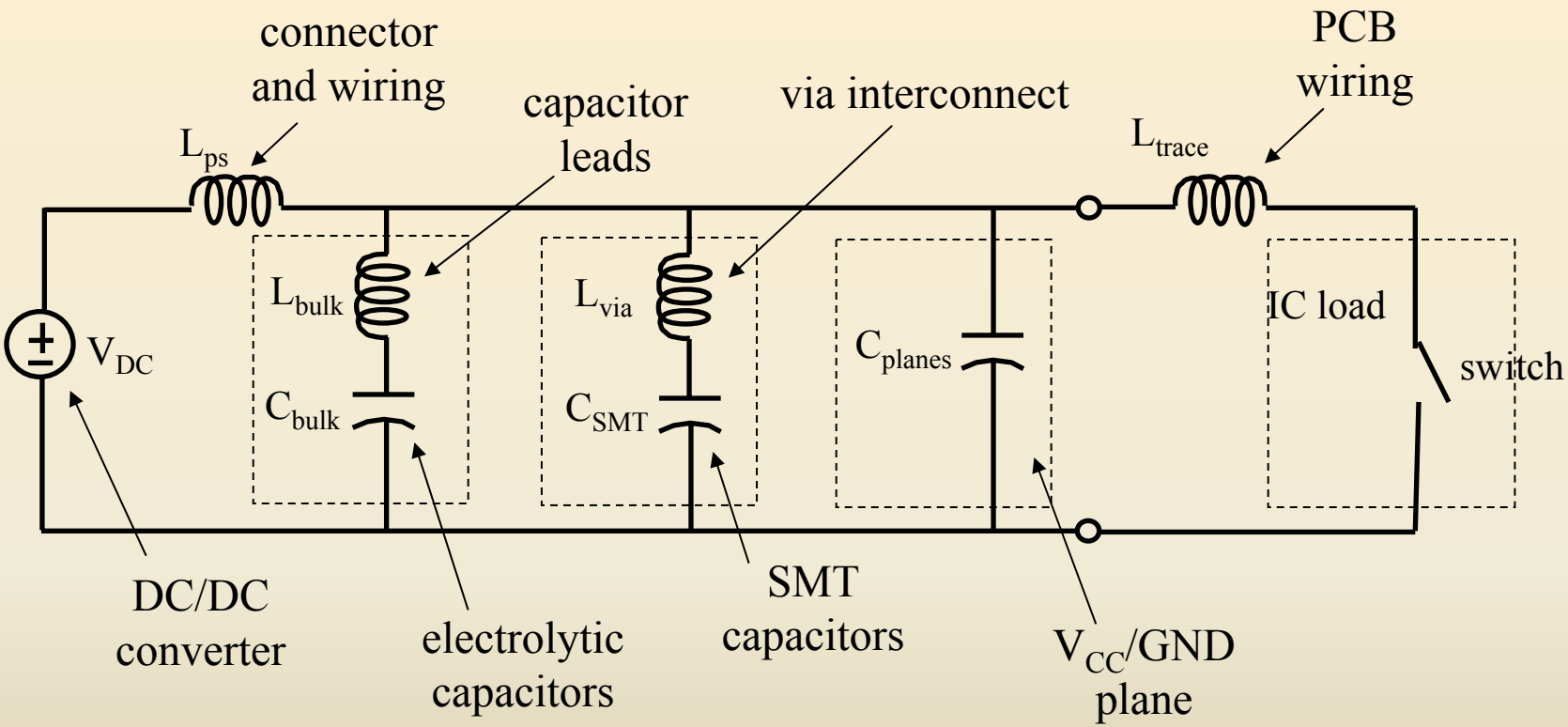




Typical PCB Power Delivery

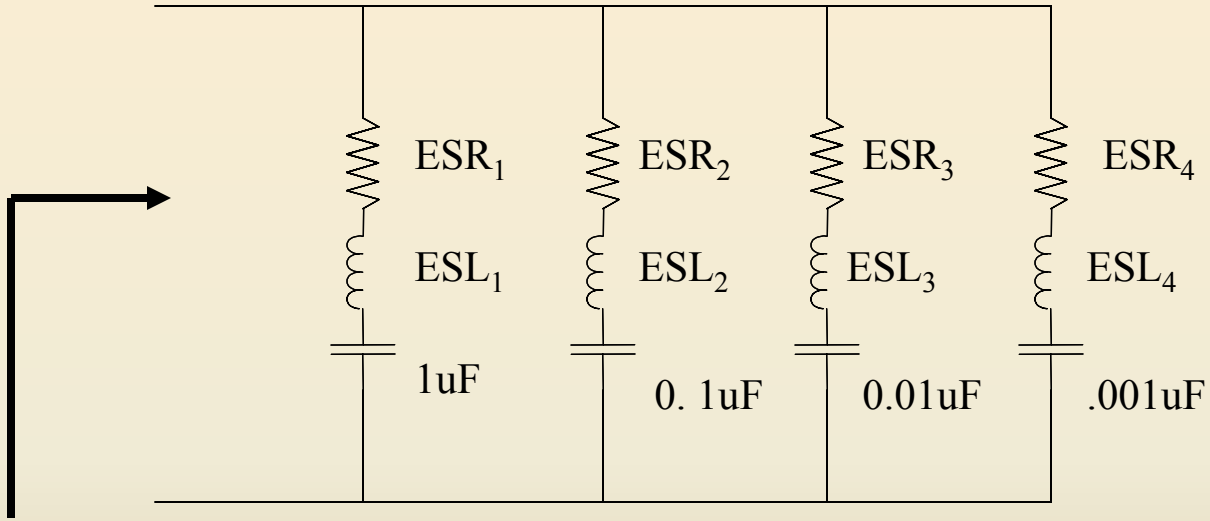


Equivalent Circuit for Power Current Delivery to IC



Traditional Analysis #1

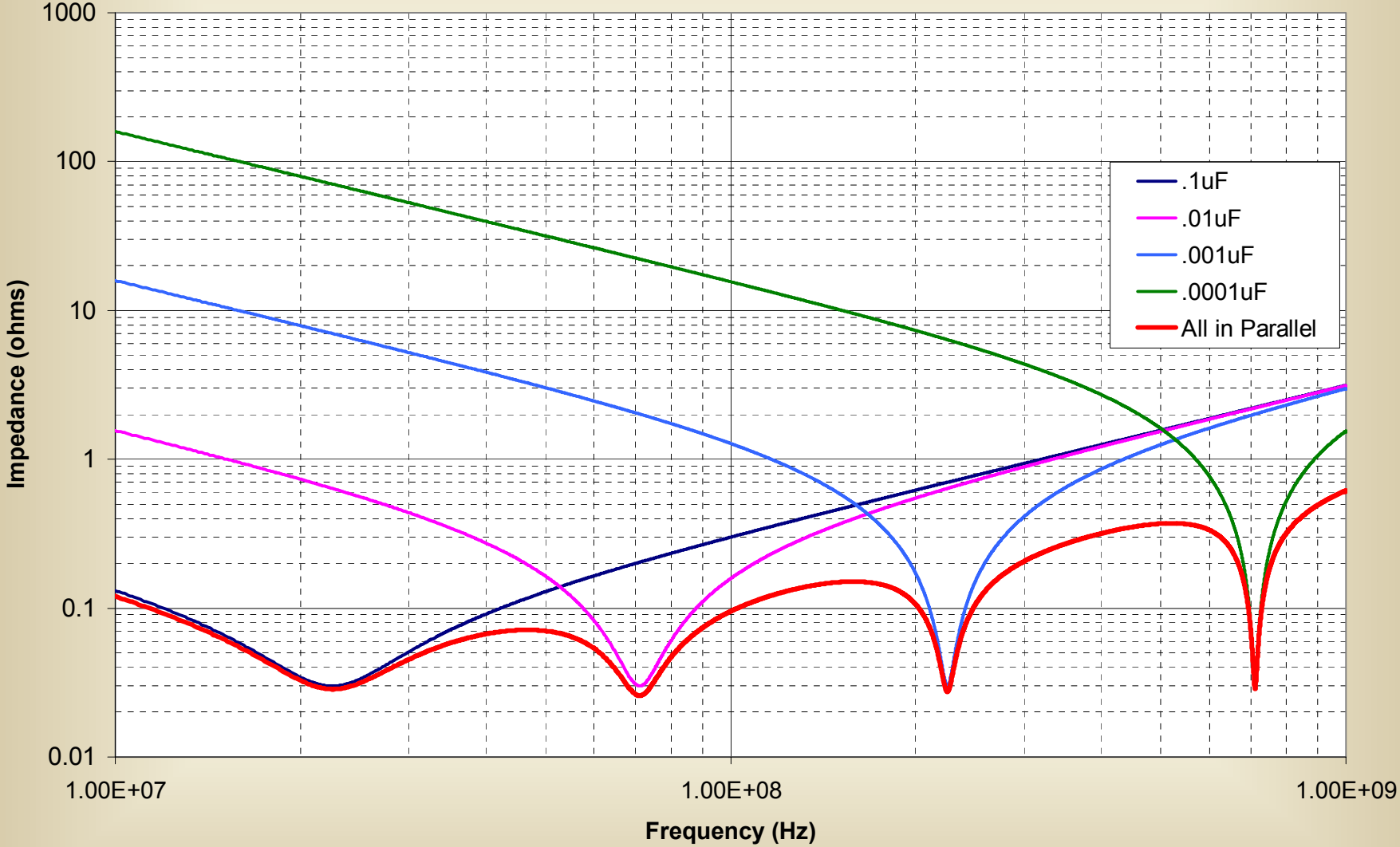
- Use impedance of capacitors in parallel



Impedance to IC power/gnd pins

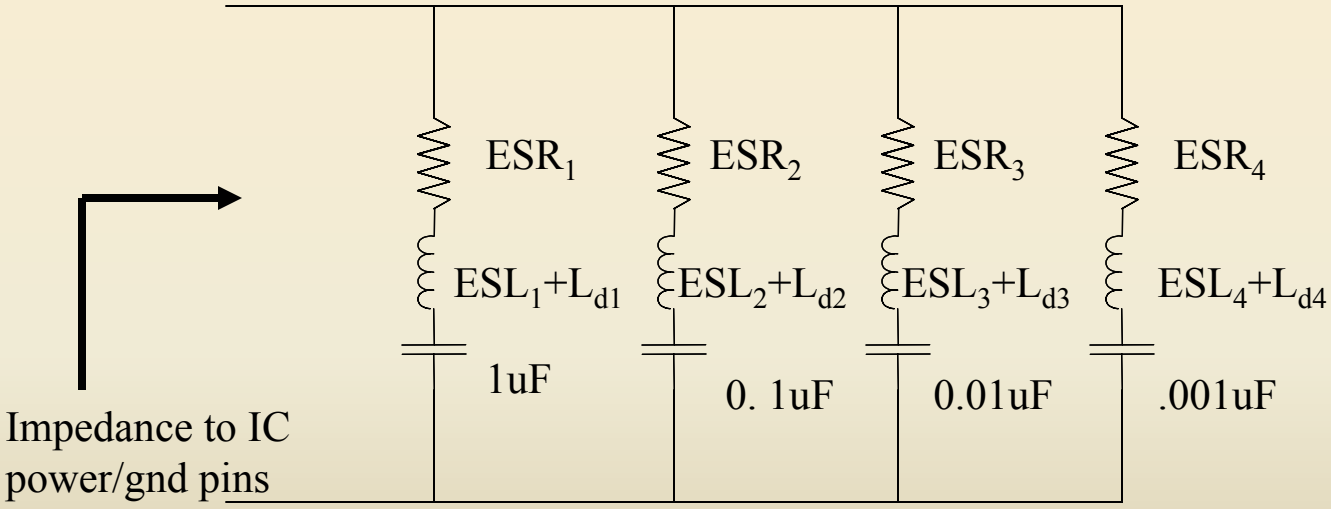
No Effect of Distance Between Capacitors and IC Included!

Traditional Impedance Calculation for Four Decoupling Capacitor Values



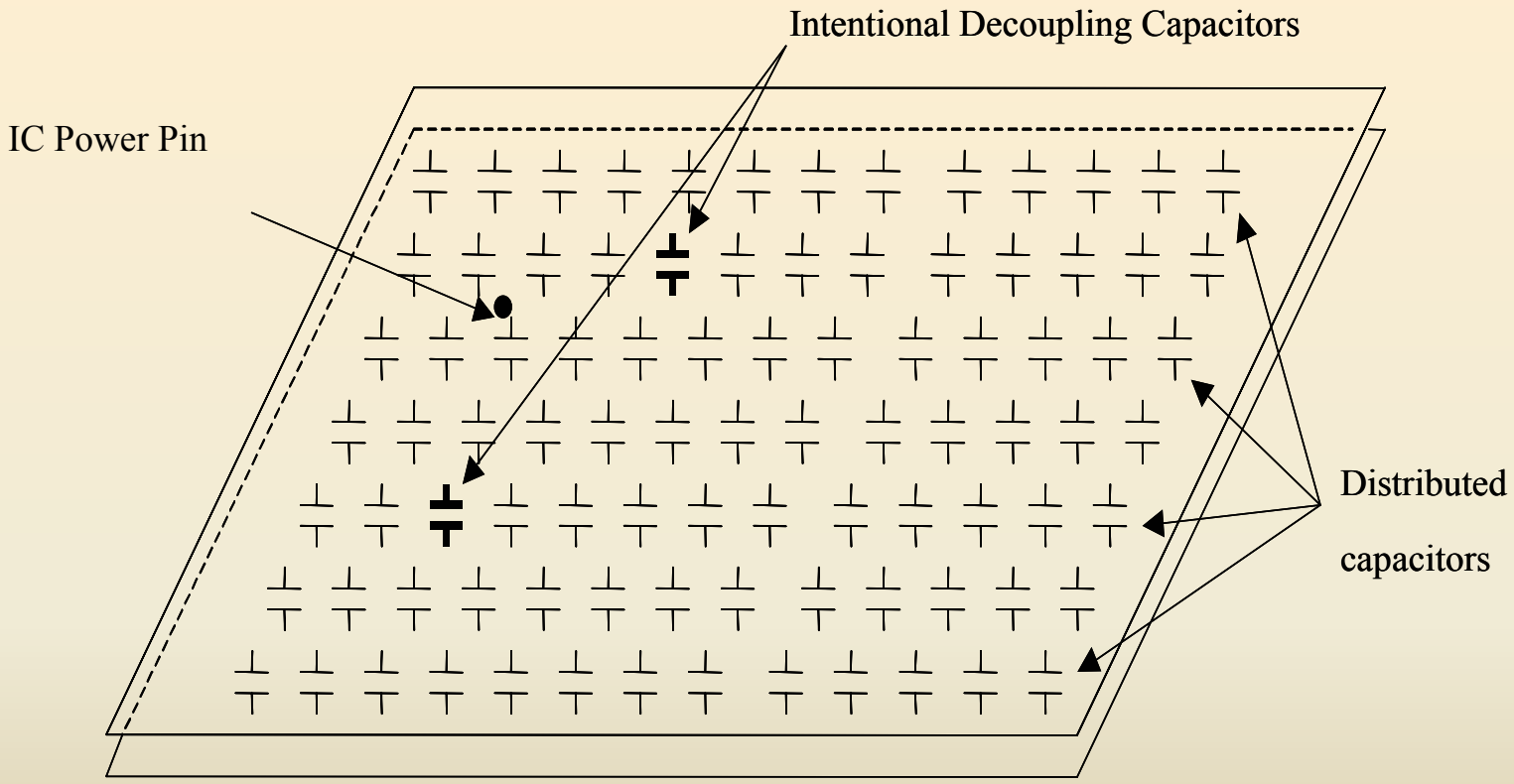
Traditional Analysis #2

- Calculate loop area – Traditional loop Inductance formulas
  - Which loop area? Which size conductor

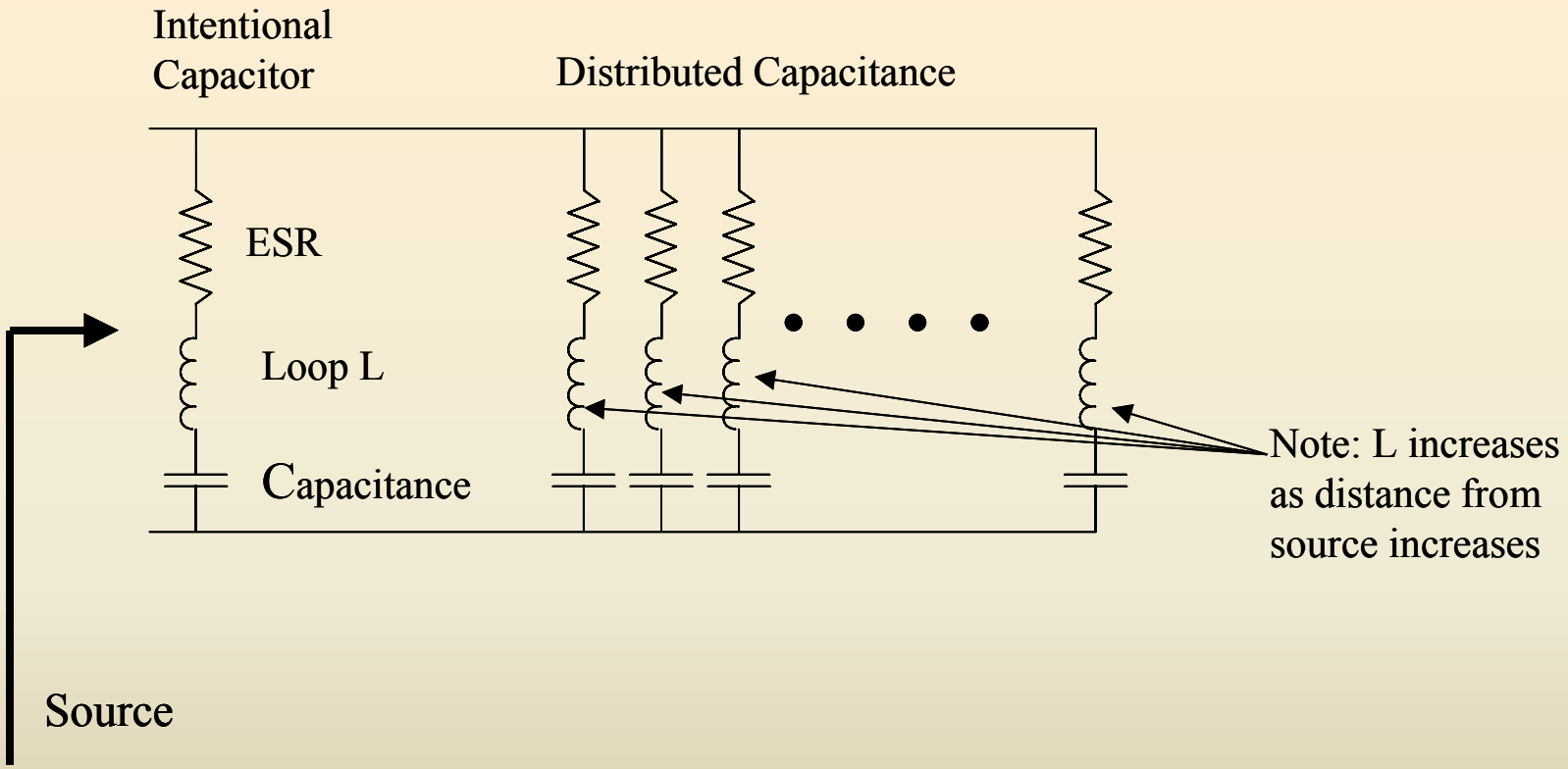


Over Estimates L and Ignores Distributed Capacitance

More Accurate Model Includes Distributed Capacitance



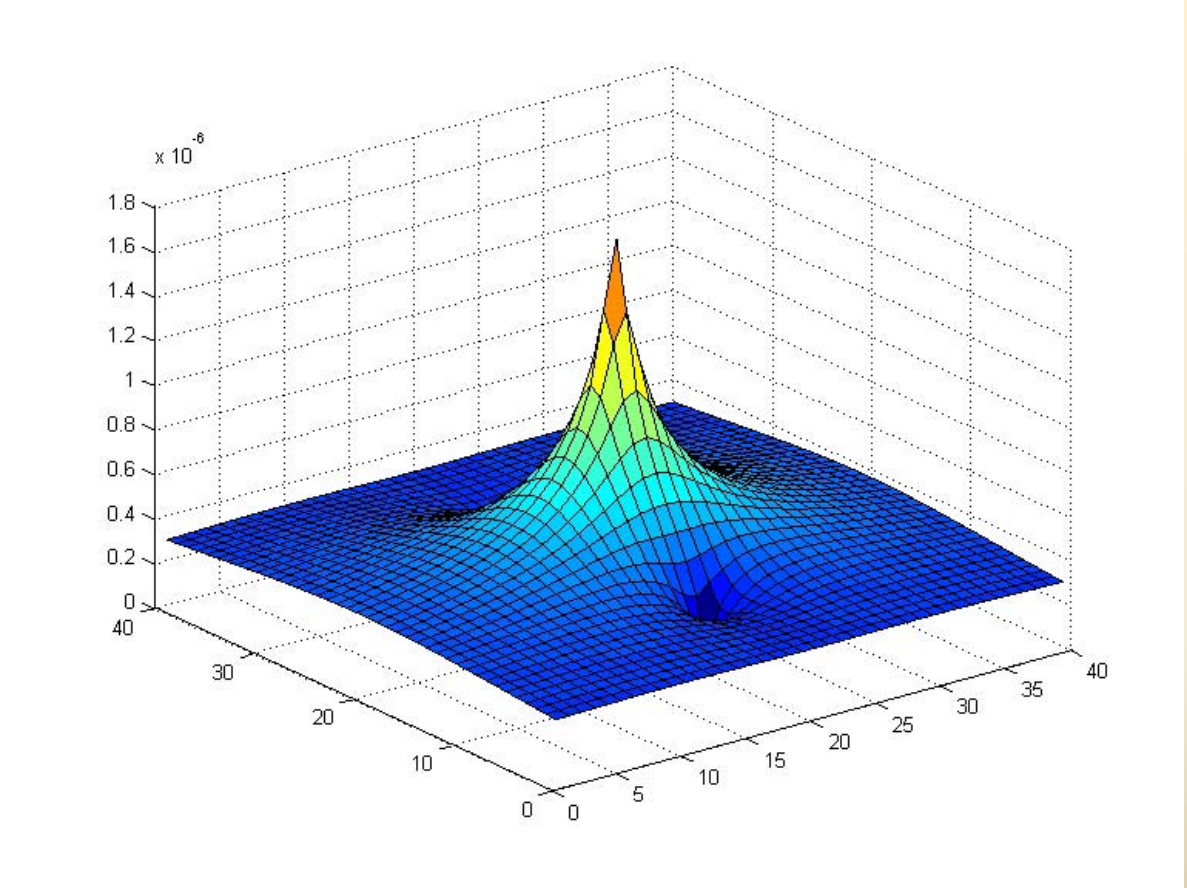
Distributed Capacitance Schematic



Effect of Distributed Capacitance

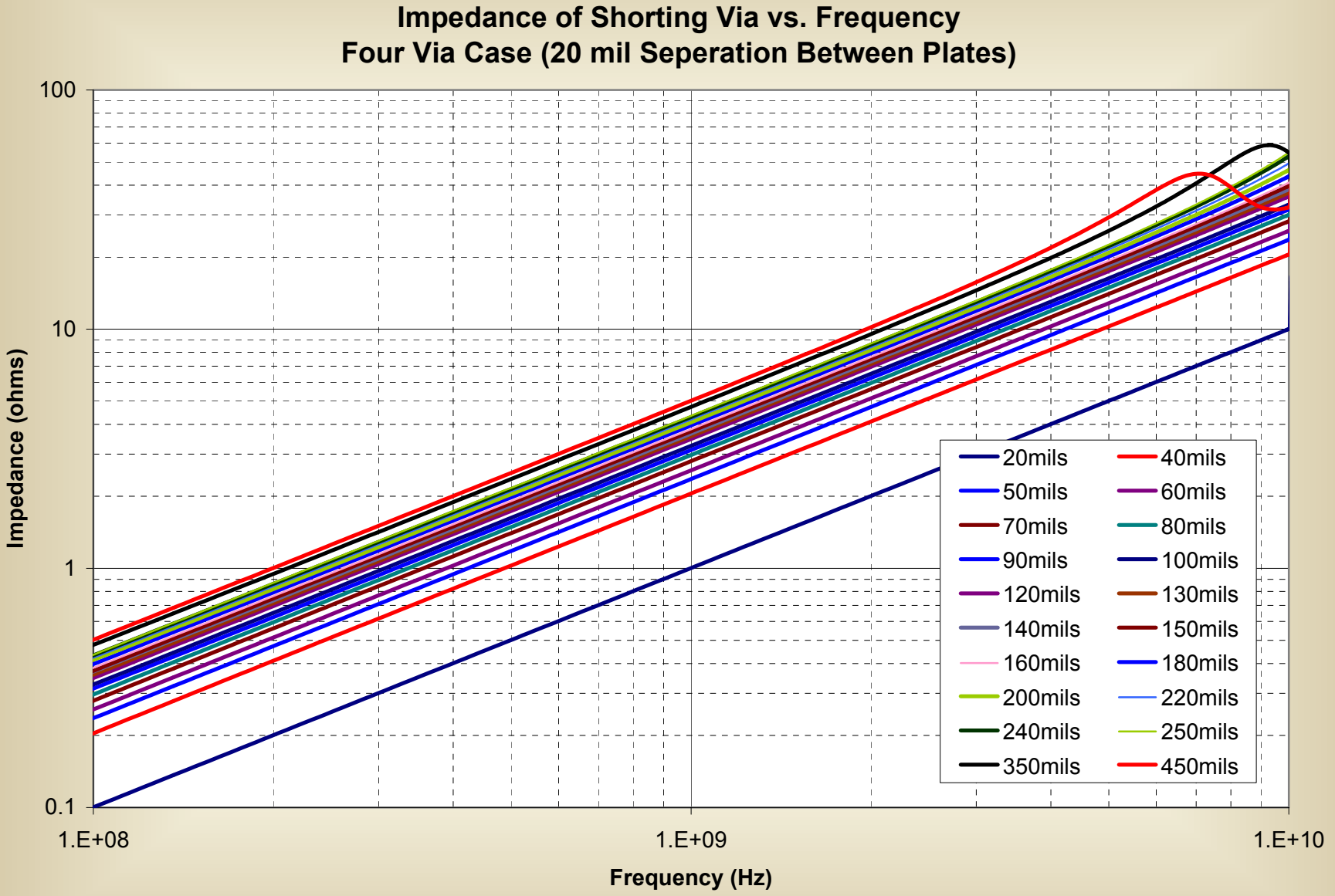
- Can NOT be calculated/estimated using traditional capacitance equation
- Displacement current amplitude changes with position and distance from the source

Displacement Current 500 MHz via @450 mils from Source



Need to Find the Real Effect of Decoupling Capacitor Distance

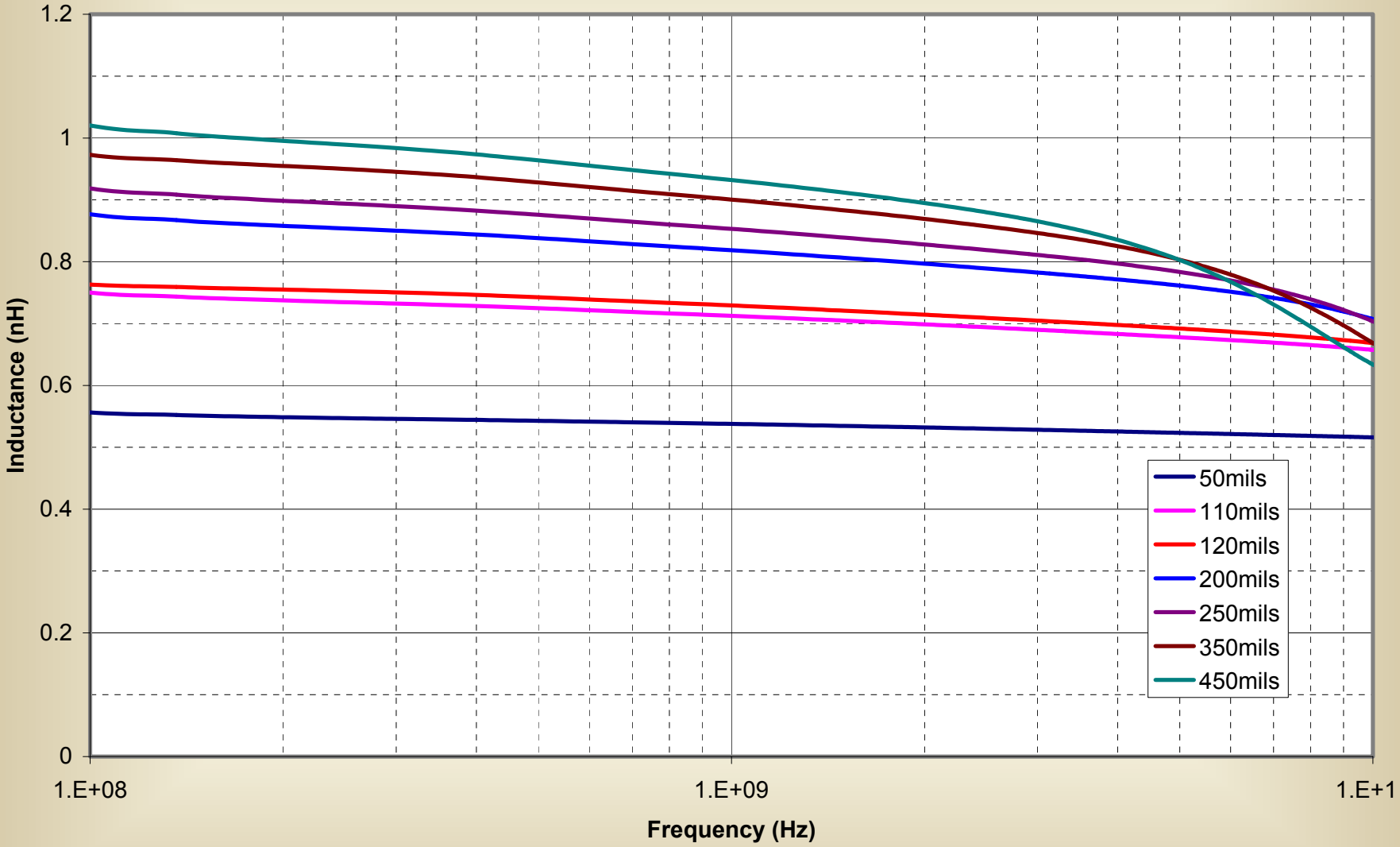
- Perfect decoupling capacitor is a via between planes
- FDTD simulation to find the effect of shorting via distance from source
- Vary spacing between planes, distance to via, frequency, etc


Impedance of Shorting Via vs. Frequency
Four Via Case (20 mil Seperation Between Plates)
Impedance (ohms)
100
10
1
0.1
1.E+08
1.E+09
1.E+10
Frequency (Hz)
20mils
40mils
50mils
60mils
70mils
80mils
90mils
100mils
120mils
130mils
140mils
150mils
160mils
180mils
200mils
220mils
240mils
250mils
350mils
450mils

Impedance Result

- Linear with frequency (on log scale)
- Looks like an inductance only!
- Consider this inductance an **Apparent Inductance**
- Apparent inductance is constant with frequency

Apparent Inductance for One Shorting Via Case
20 mil Plate Separation



Formulas to Predict Apparent Inductance

$$L_{one-via} = (0.1336s - 0.0654)Ln(dist) + (-0.2609s + 0.2675)$$

$$L_{two-via} = (0.1307s - 0.0492)Ln(dist) + (-0.2948s + 0.1943)$$

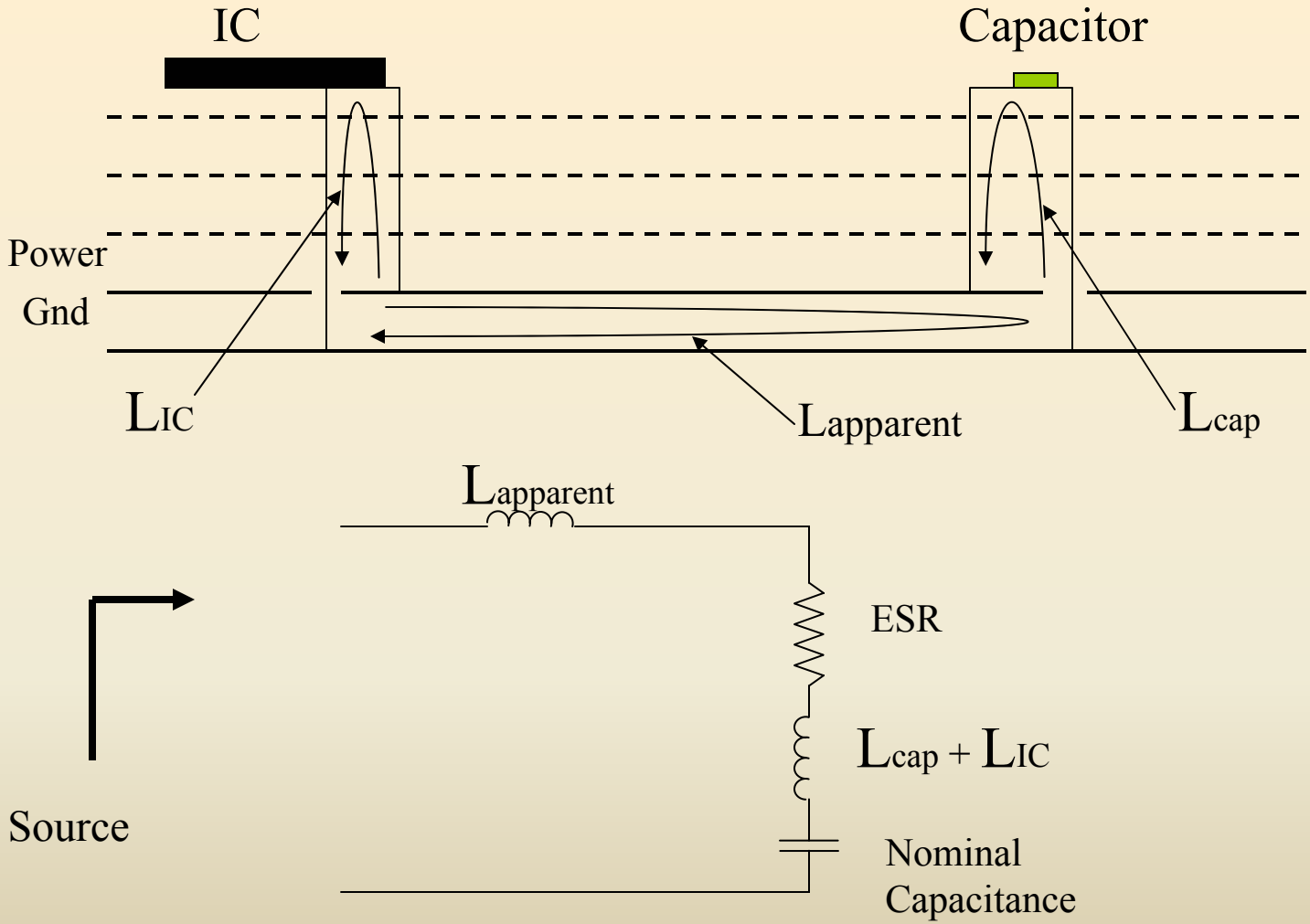
$$L_{three-via} = (0.1242s - 0.0447)Ln(dist) + (-0.2848s + 0.1763)$$

$$L_{four-via} = (0.1192s - 0.0403)Ln(dist) + (-0.2774s + 0.1592)$$

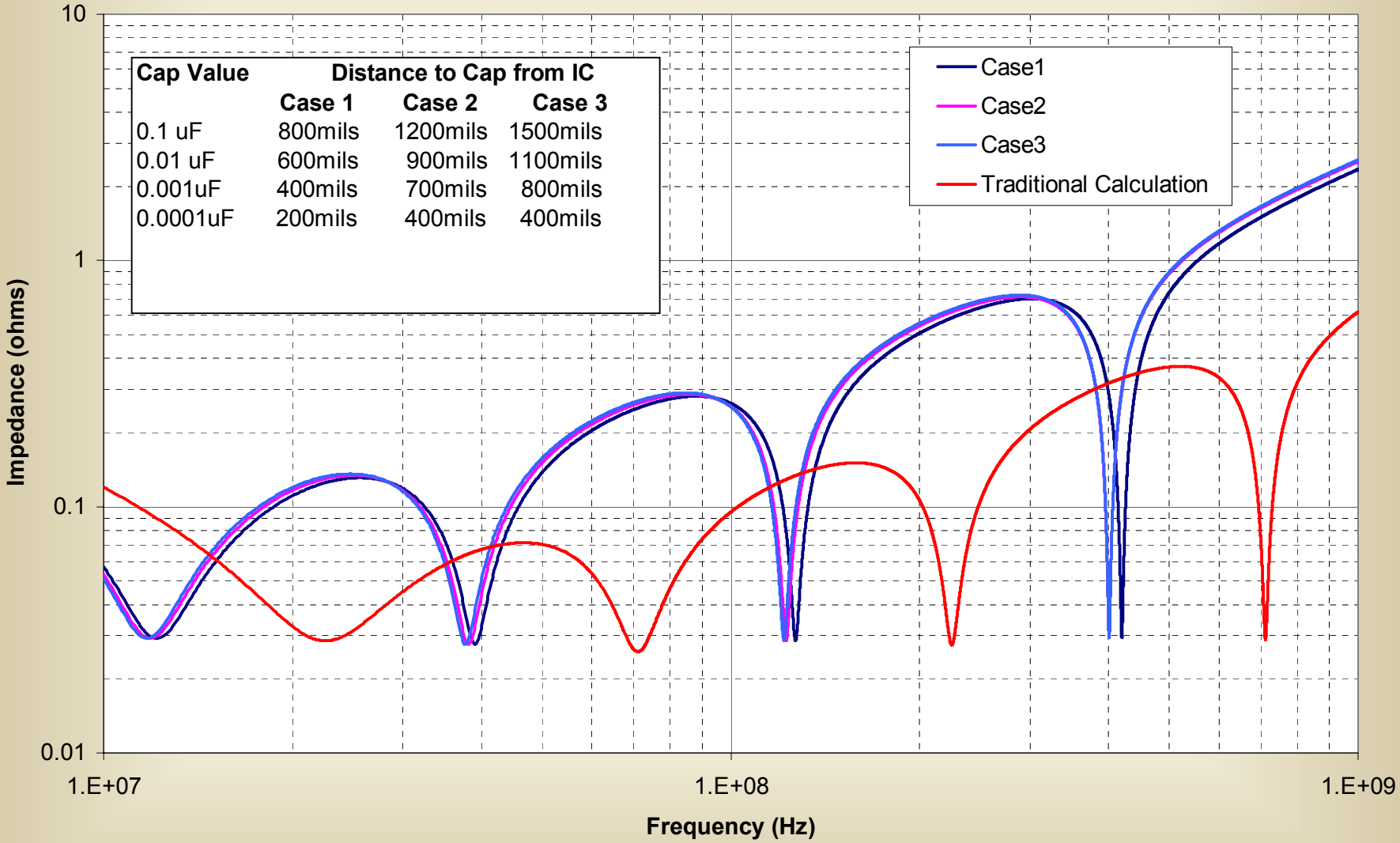
s = separation between plates (mils/10)

$dist$ = distance to via

True Impedance for Decoupling Capacitor



Impedance Calculation with Apparent Inductance for Four Decoupling Capacitor Values

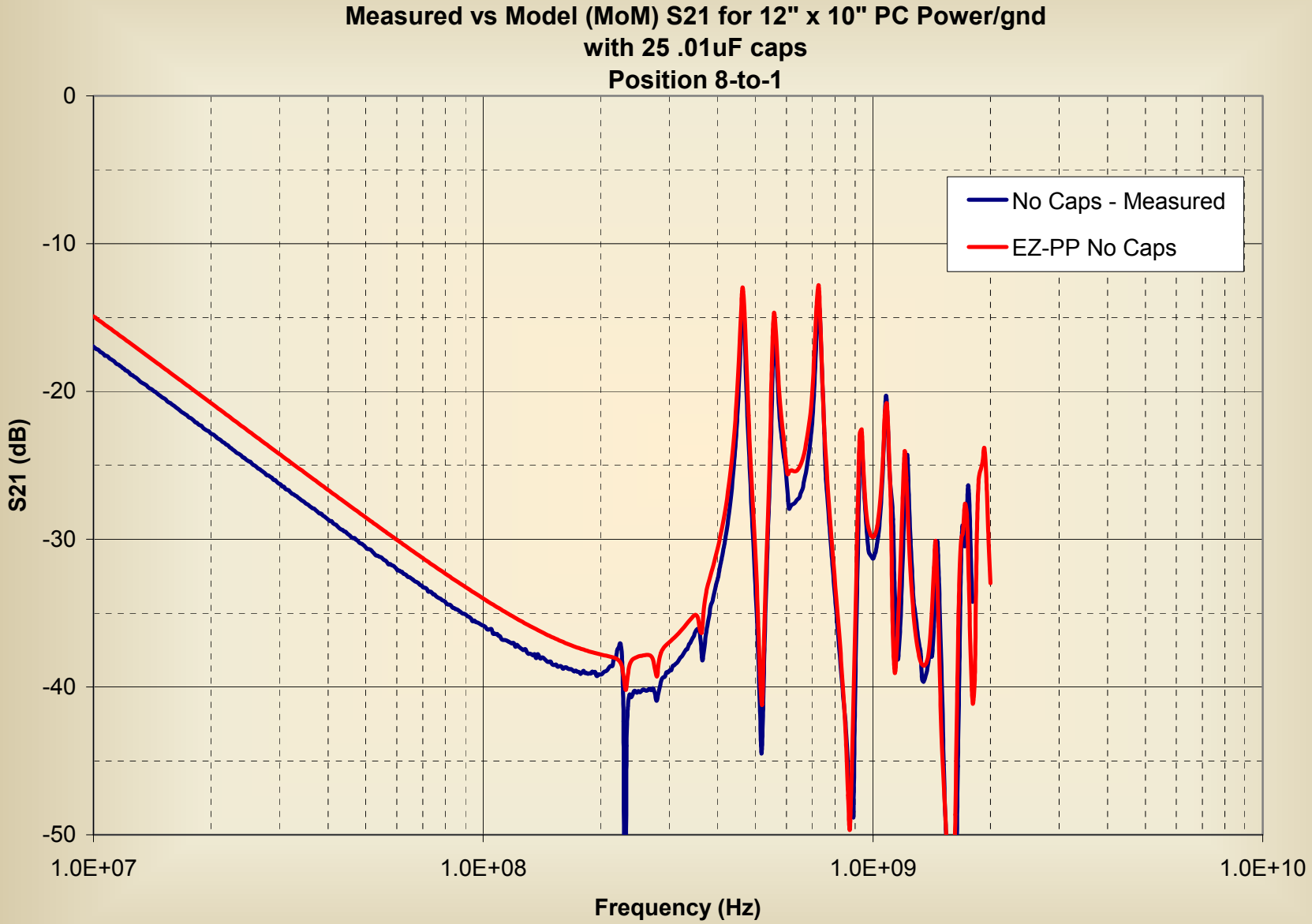


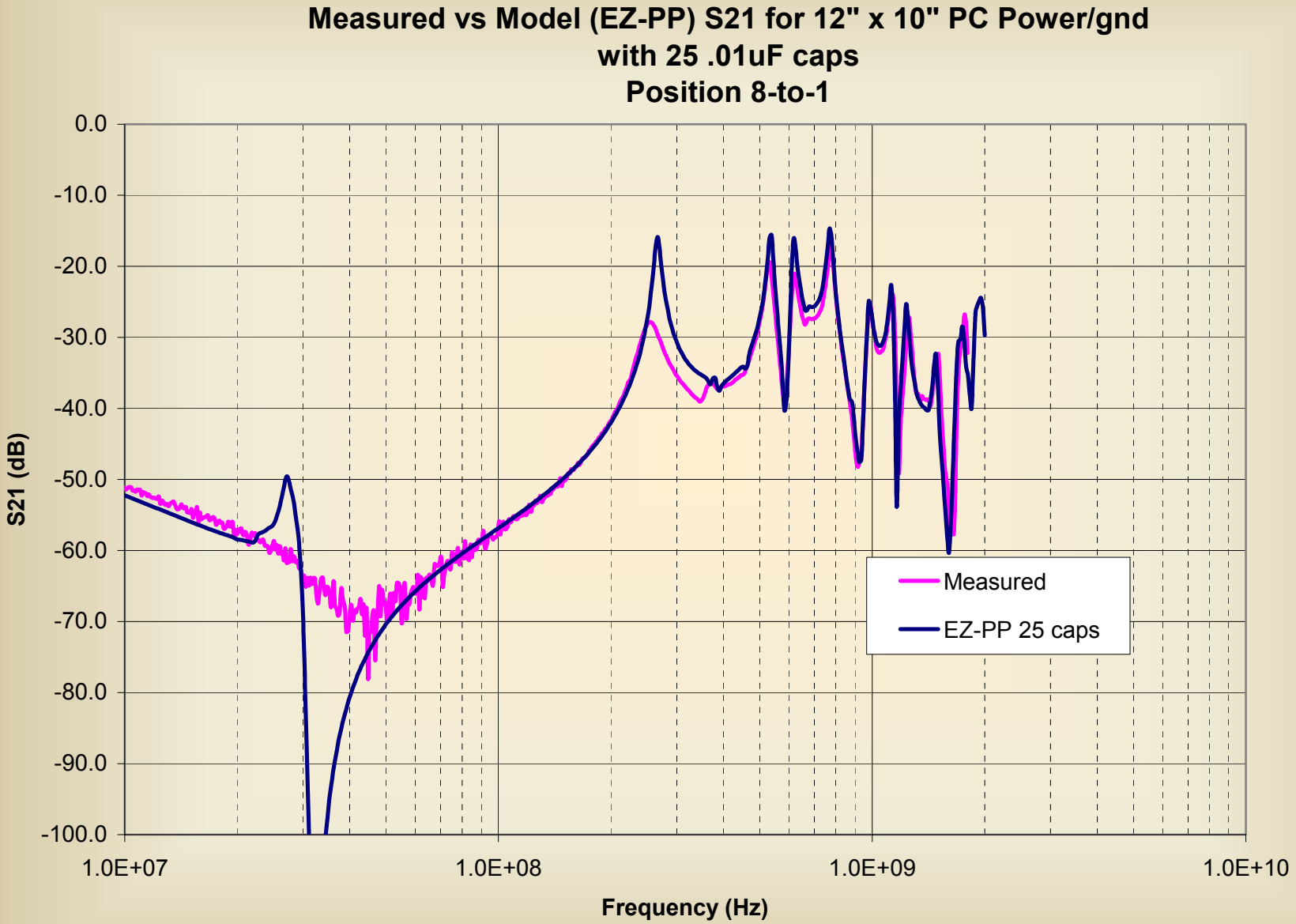
Effect of Distributed Capacitance

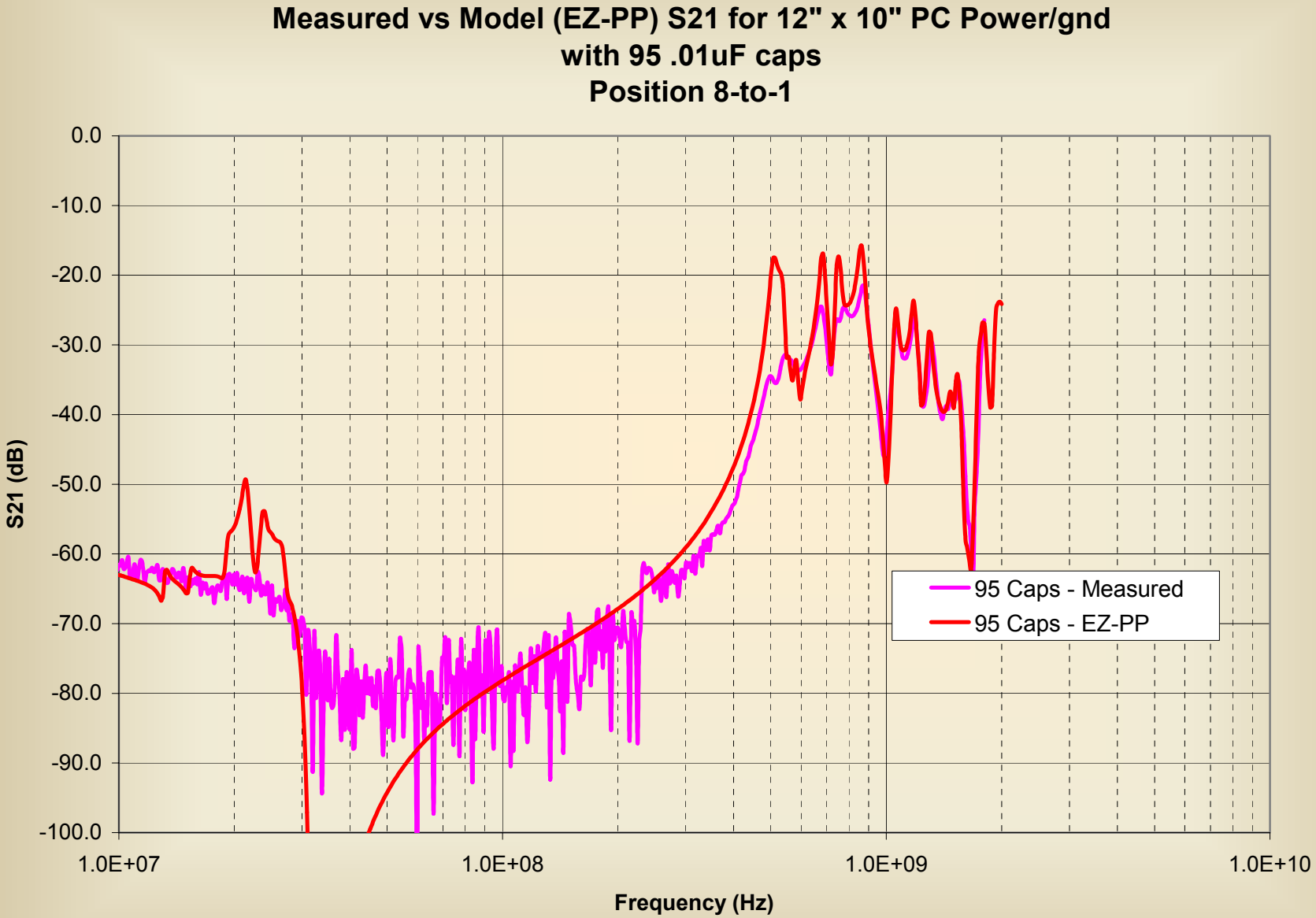
- Can NOT be calculated/estimated using traditional capacitance equation
- Displacement current amplitude changes with position and distance from the source
- Following examples use cavity resonance technique (EZ-PowerPlane)
  - Frequency Domain to compare to measurements
  - Time Domain using SPICE circuit from cavity resonance analysis

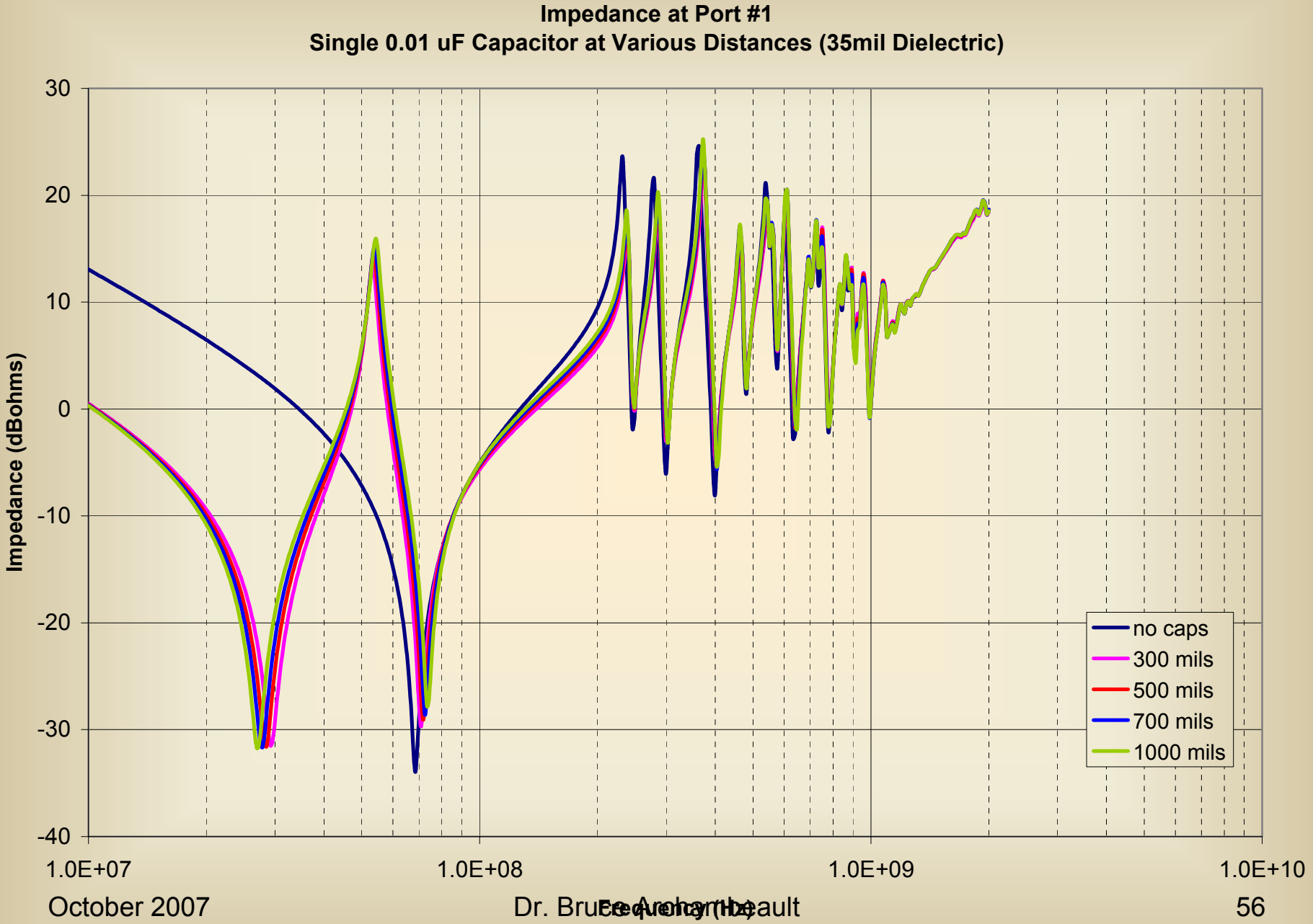
Parameters for Comparison to Measurements

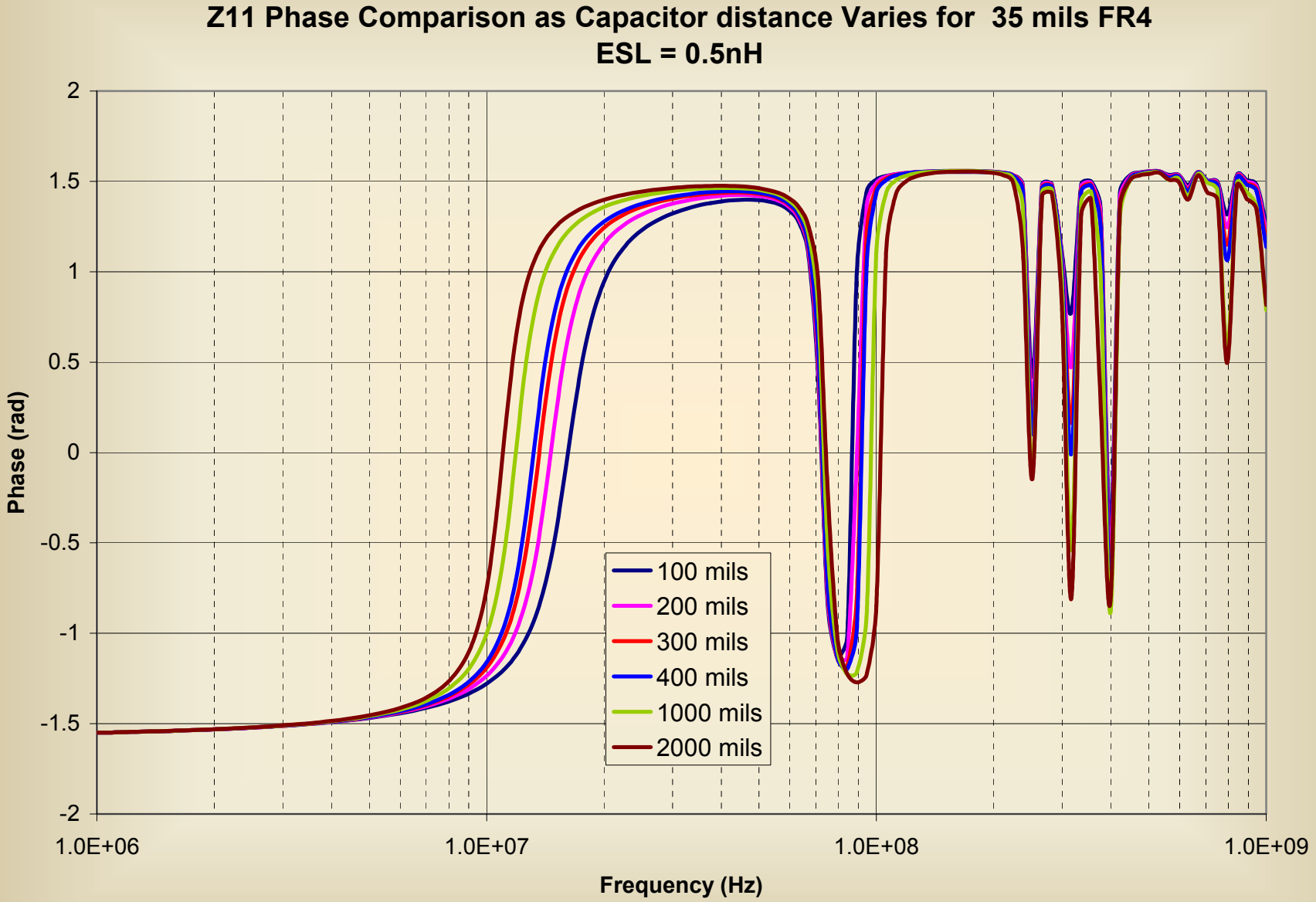
- Dielectric thickness = 35 mils
- Dielectric constant = 4.5, Loss tan = 0.02
- Copper conductivity = 5.8 e7 S/m

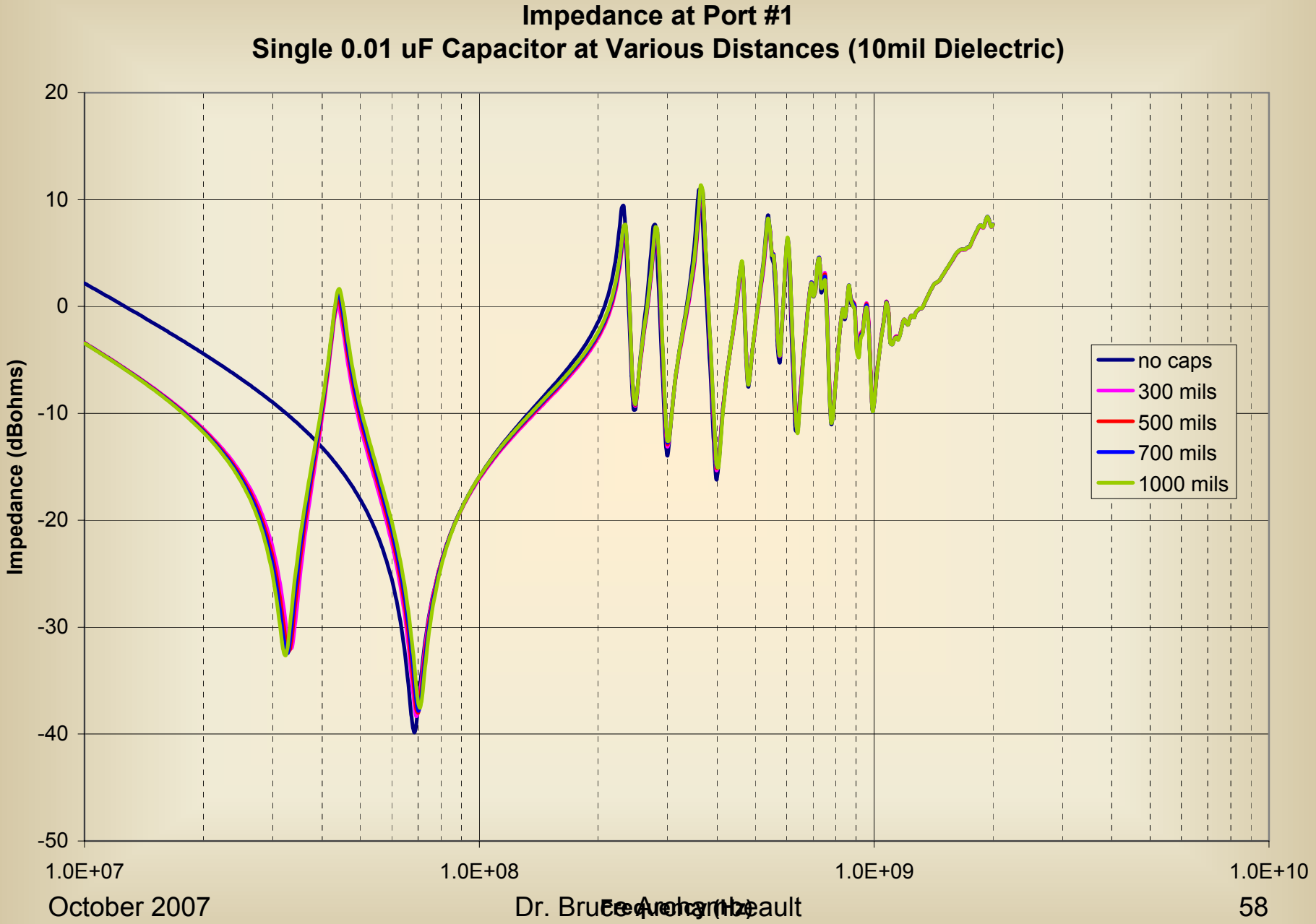

Measured vs Model (MoM) S21 for 12" x 10" PC Power/gnd
with 25 .01uF caps
Position 8-to-1
0
-10
-20
-30
-40
-50
S21 (dB)
No Caps - Measured
EZ-PP No Caps
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)


Measured vs Model (EZ-PP) S21 for 12" x 10" PC Power/gnd
with 25 .01uF caps
Position 8-to-1
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
S21 (dB)
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
Measured
EZ-PP 25 caps

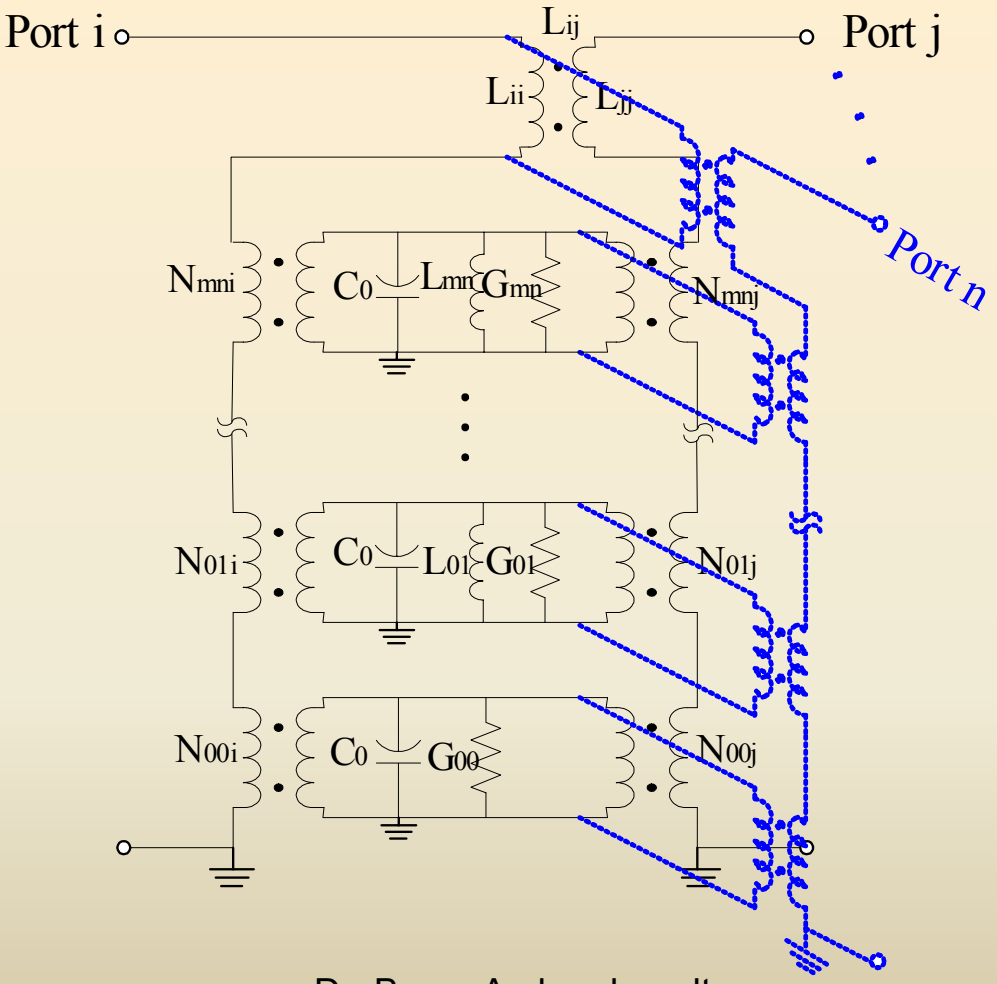

Measured vs Model (EZ-PP) S21 for 12" x 10" PC Power/gnd
with 95 .01uF caps
Position 8-to-1
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
S21 (dB)
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
95 Caps - Measured
95 Caps - EZ-PP


Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (35mil Dielectric)
Impedance (dBohms)
30
20
10
0
-10
-20
-30
-40
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
no caps
300 mils
500 mils
700 mils
1000 mils

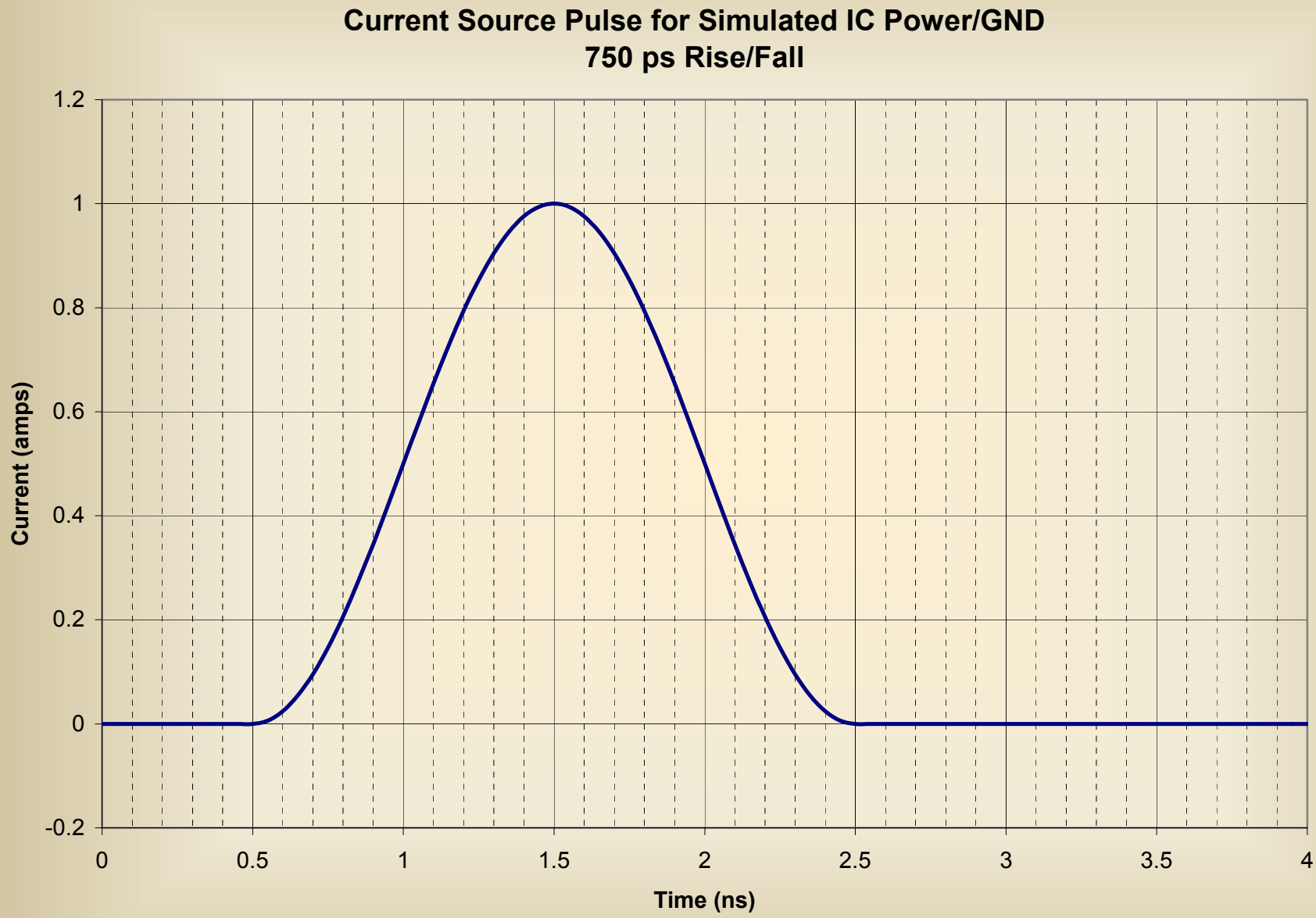

Z11 Phase Comparison as Capacitor distance Varies for 35 mils FR4
ESL = 0.5nH
Phase (rad)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
1.0E+06
1.0E+07
1.0E+08
1.0E+09
Frequency (Hz)
100 mils
200 mils
300 mils
400 mils
1000 mils
2000 mils


Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (10mil Dielectric)
Impedance (dBohms)
20
10
0
-10
-20
-30
-40
-50
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
no caps
300 mils
500 mils
700 mils
1000 mils

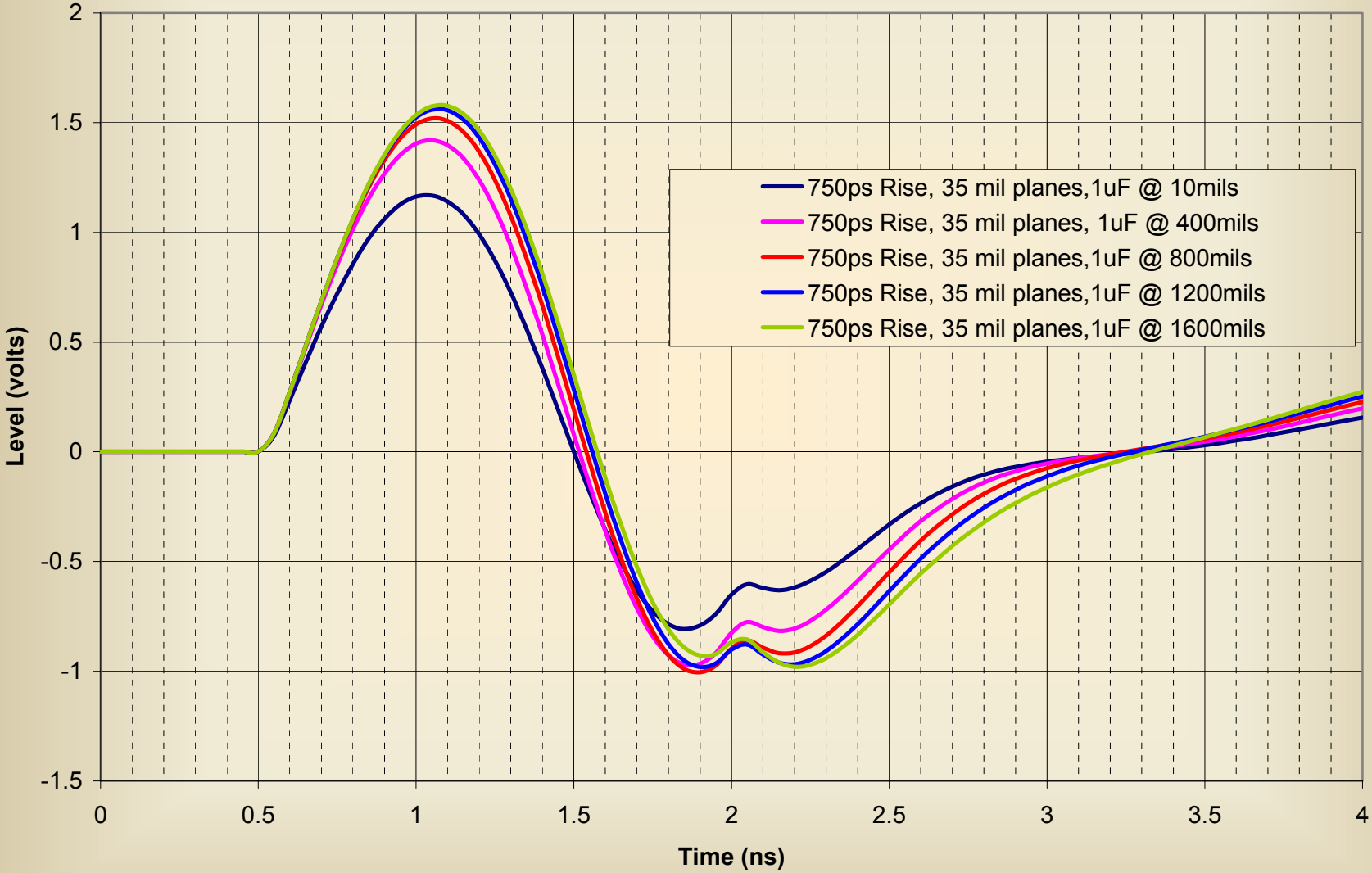
Cavity Resonance (EZ-PowerPlane) Equivalent Circuit for HSPICE

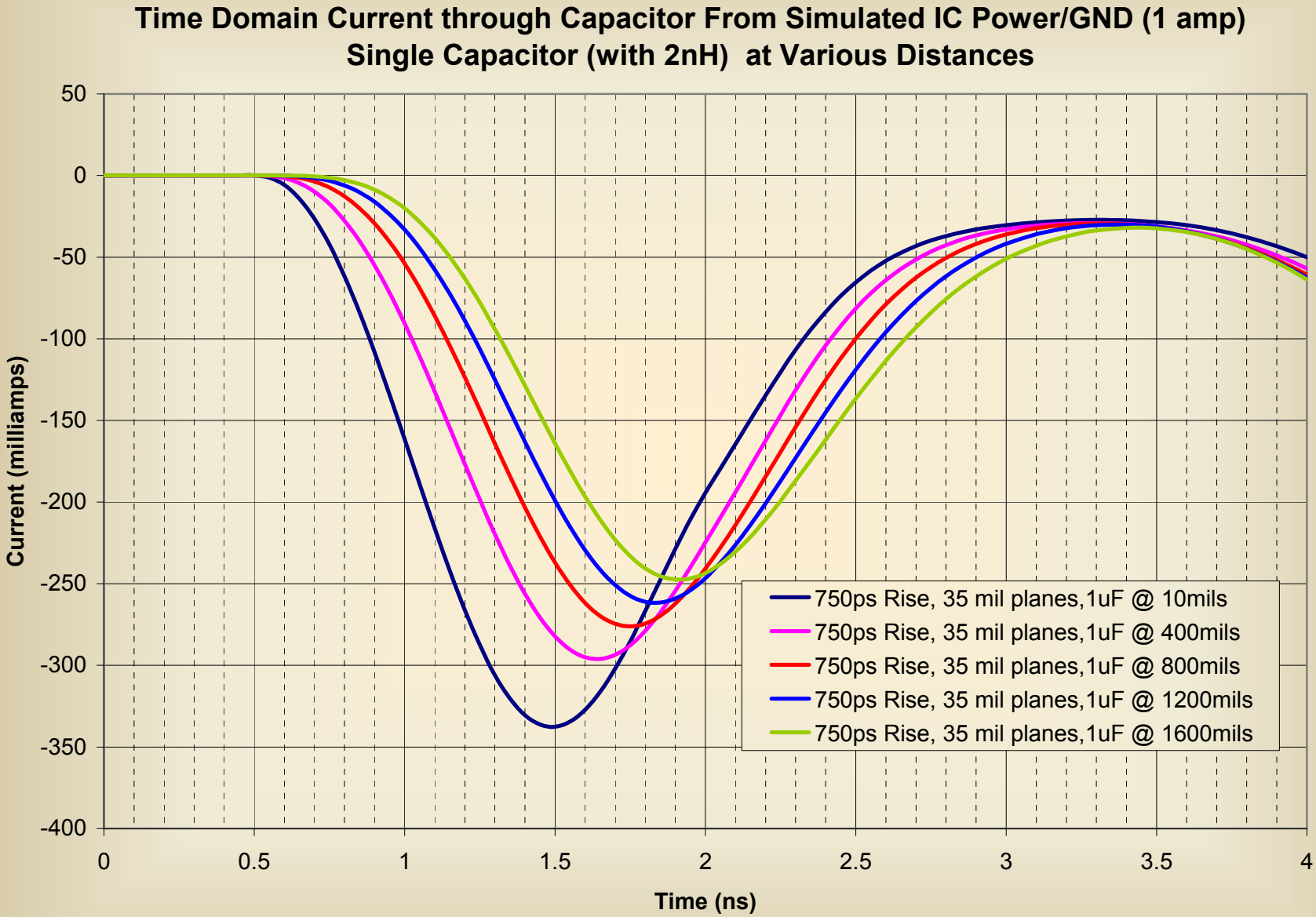


Impedance Comparison (EZ-PP vs HSPICE) at Port #1
Single 0.01 uF Capacitor at Various Distances (10mil Dielectric)

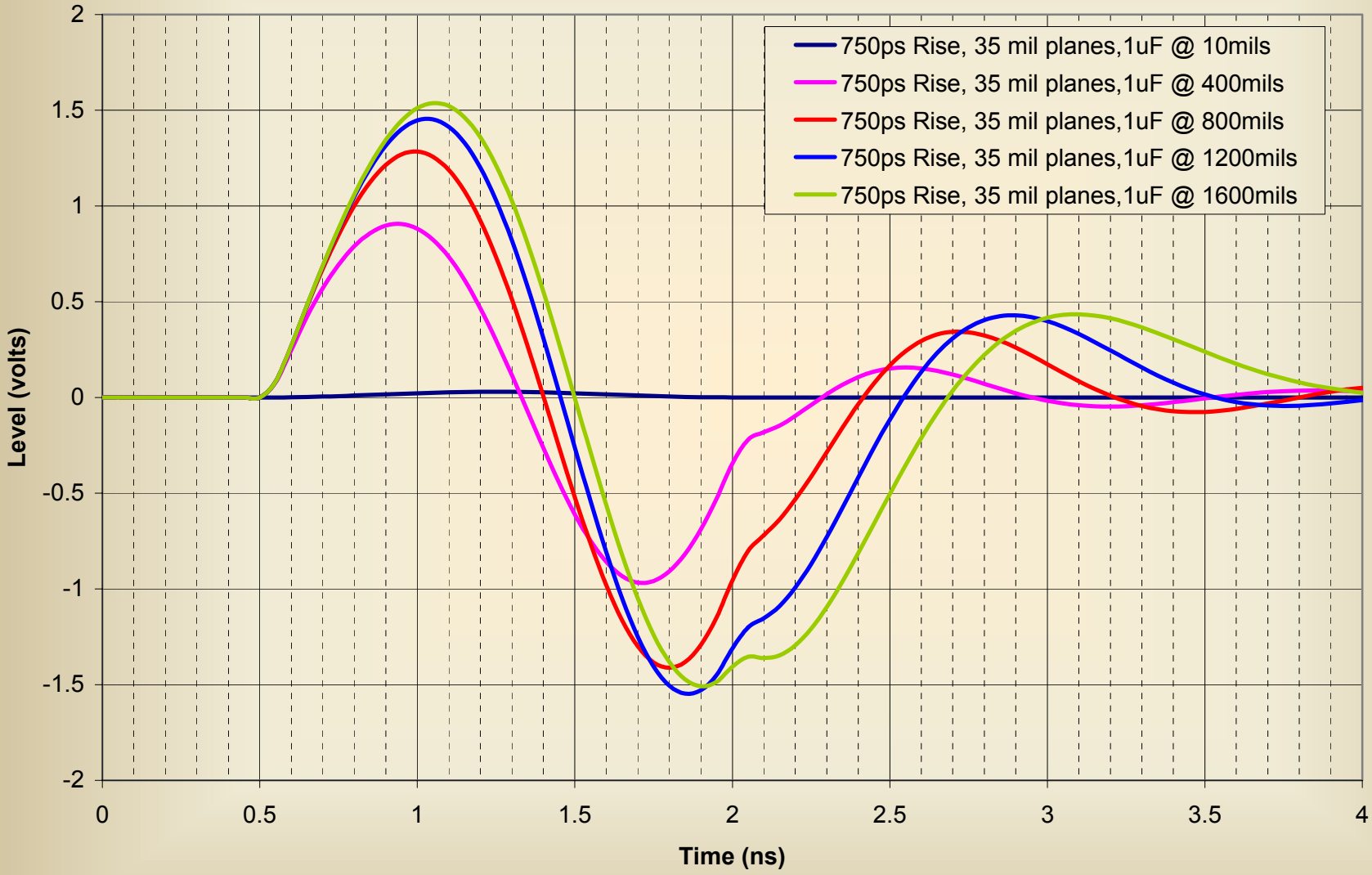

Current Source Pulse for Simulated IC Power/GND
750 ps Rise/Fall
Current (amps)
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
0.5
1
1.5
2
2.5
3
3.5
4
Time (ns)

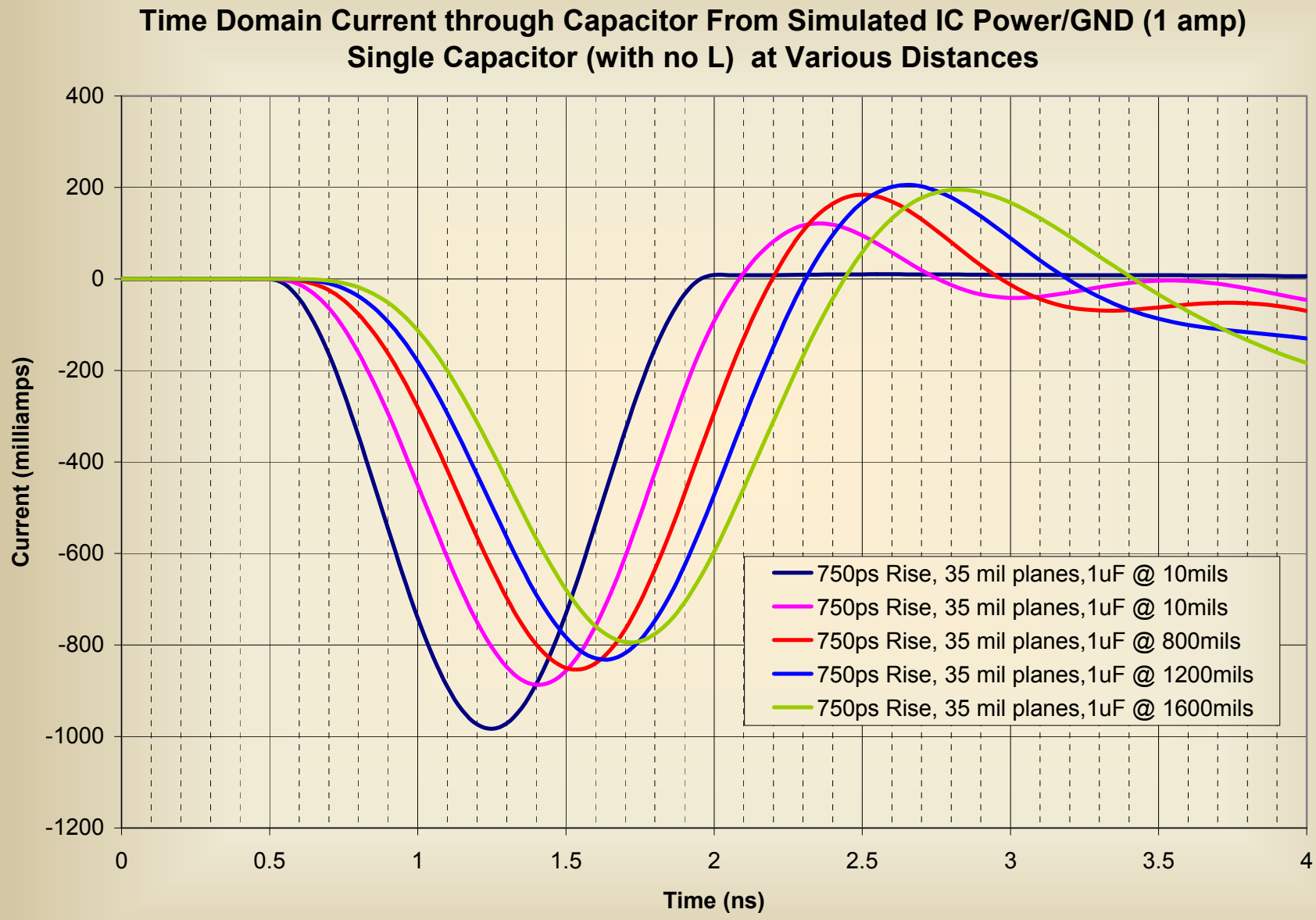
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp) Single Capacitor (with 2 nH) at Various Distances (Fullwave Simulation)



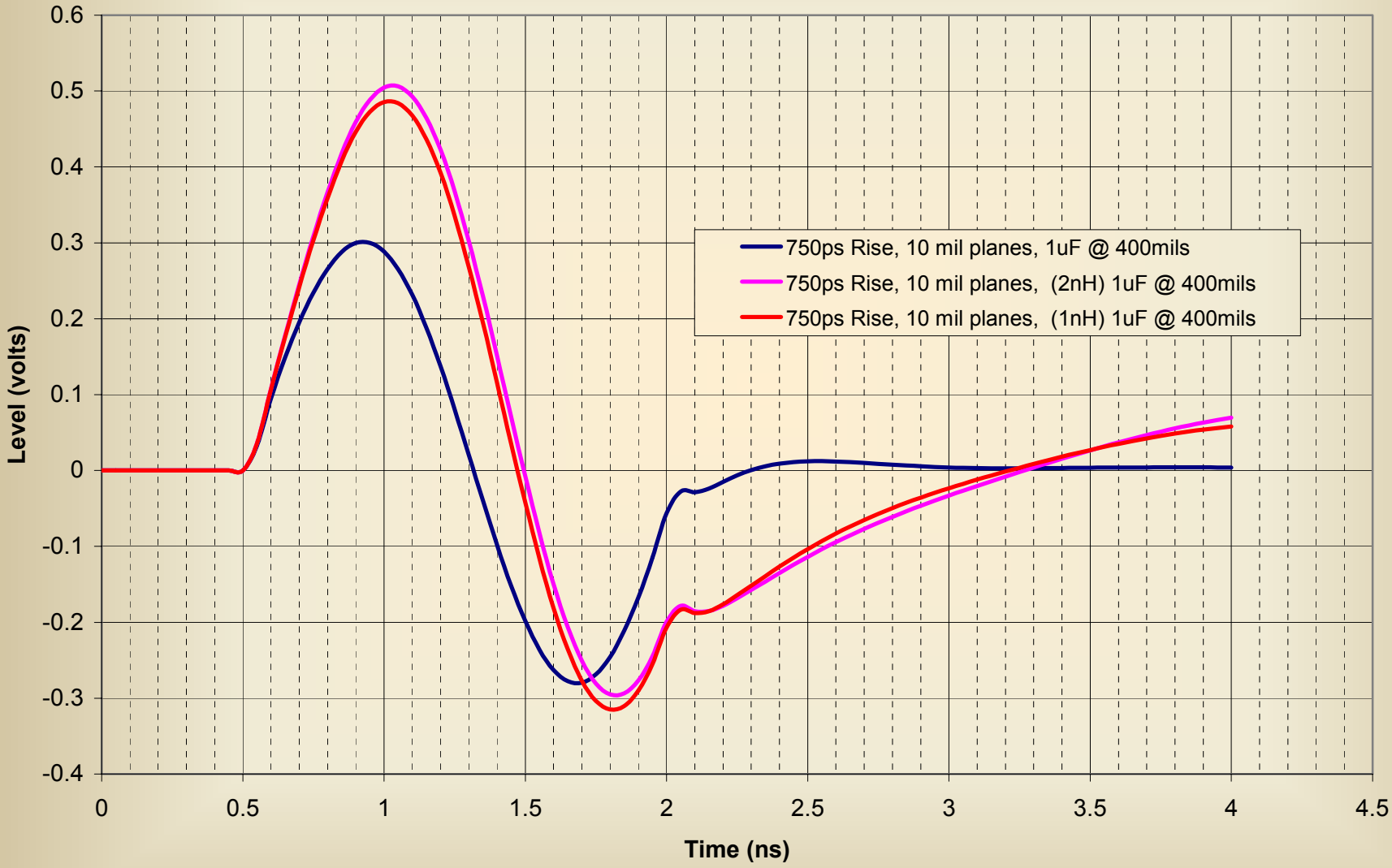

Time Domain Current through Capacitor From Simulated IC Power/GND (1 amp)
Single Capacitor (with 2nH) at Various Distances
Current (milliamps)
50
0
-50
-100
-150
-200
-250
-300
-350
-400
0
0.5
1
1.5
2
2.5
3
3.5
4
Time (ns)
750ps Rise, 35 mil planes,1uF @ 10mils
750ps Rise, 35 mil planes,1uF @ 400mils
750ps Rise, 35 mil planes,1uF @ 800mils
750ps Rise, 35 mil planes,1uF @ 1200mils
750ps Rise, 35 mil planes,1uF @ 1600mils

Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with No L) at Various Distances

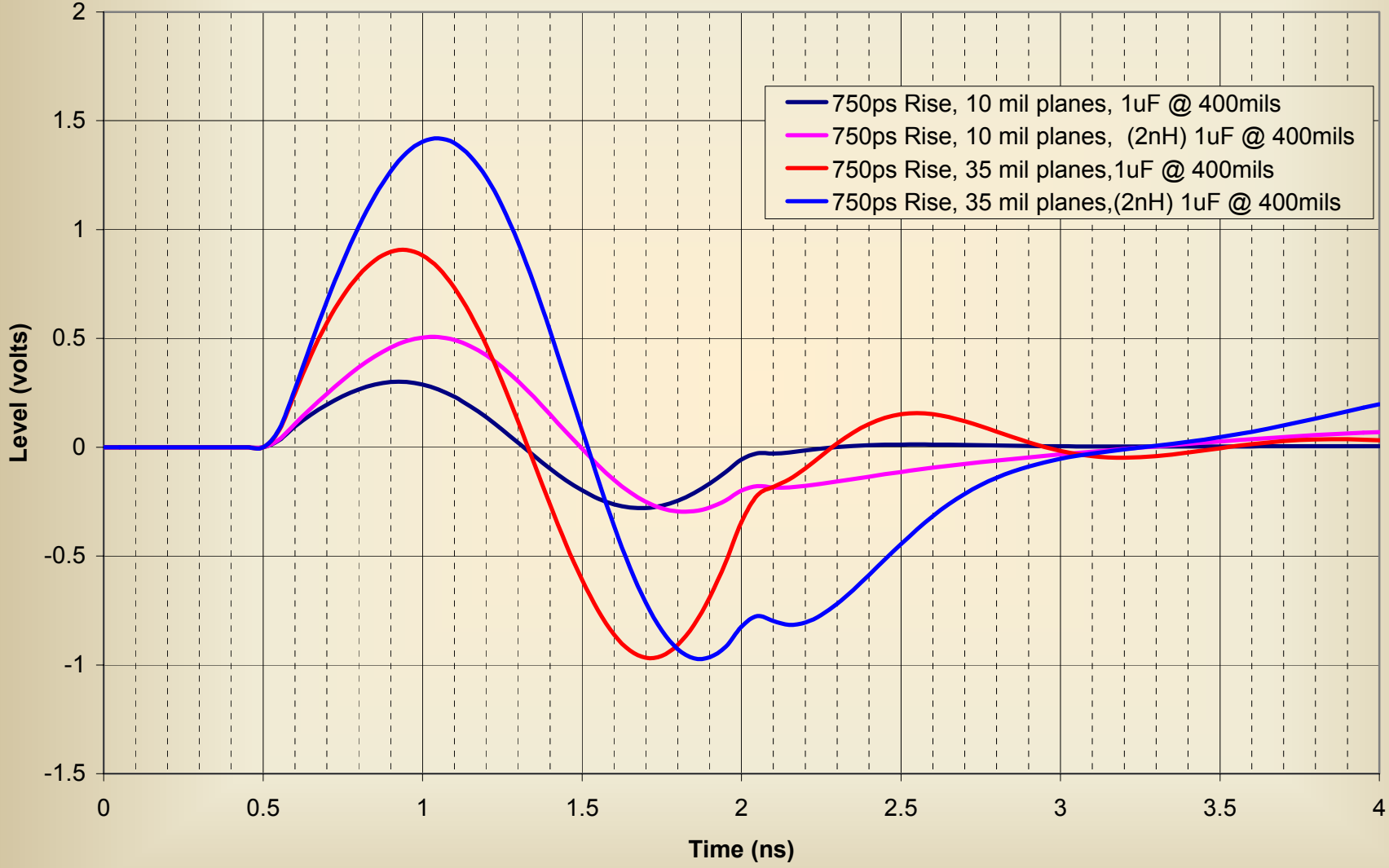



Time Domain Current through Capacitor From Simulated IC Power/GND (1 amp)
Single Capacitor (with no L) at Various Distances
Current (milliamps)
400
200
0
-200
-400
-600
-800
-1000
-1200
0
0.5
1
1.5
2
2.5
3
3.5
4
Time (ns)
750ps Rise, 35 mil planes,1uF @ 10mils
750ps Rise, 35 mil planes,1uF @ 10mils
750ps Rise, 35 mil planes,1uF @ 800mils
750ps Rise, 35 mil planes,1uF @ 1200mils
750ps Rise, 35 mil planes,1uF @ 1600mils

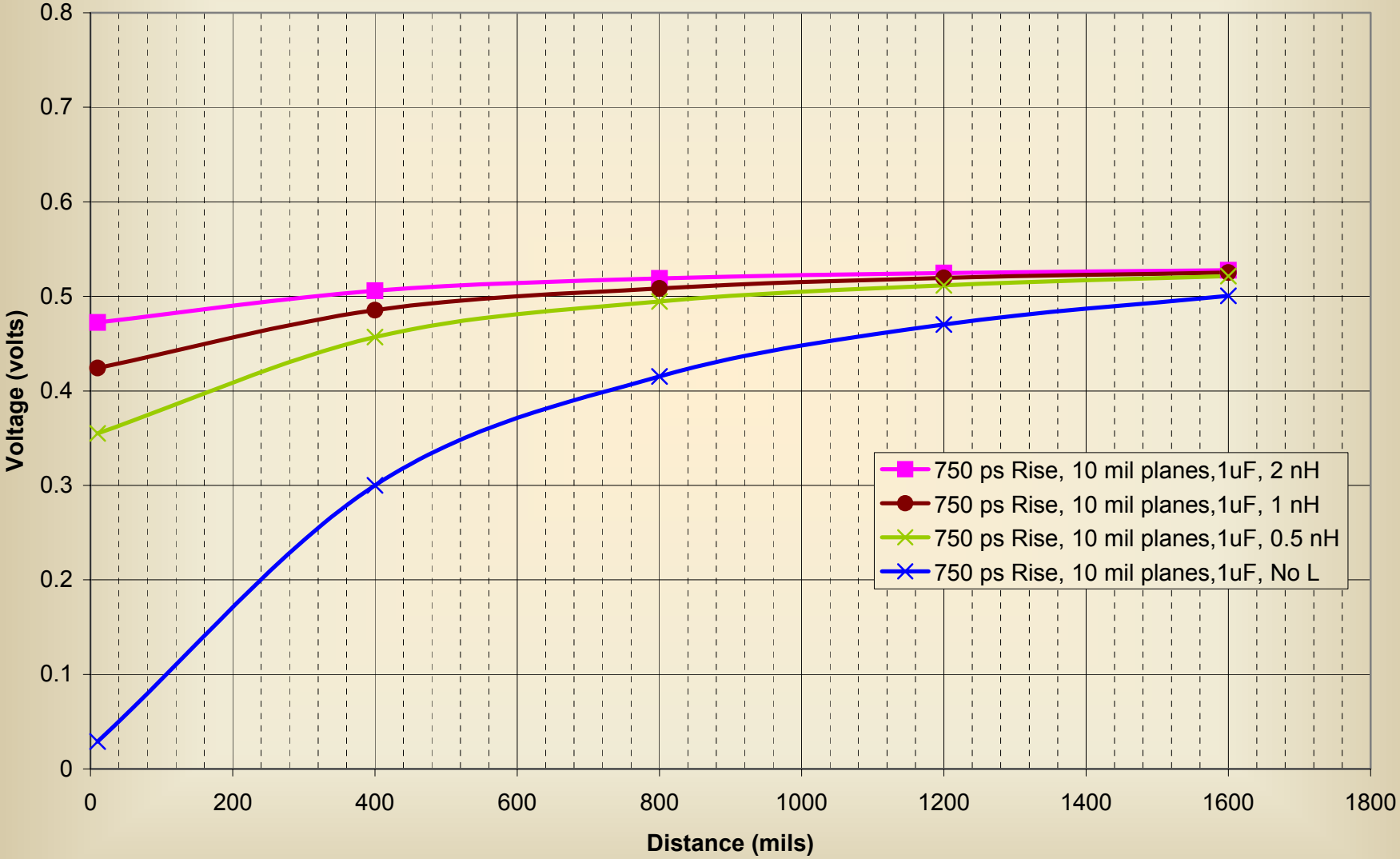
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor with Various Capacitor Connection Inductance



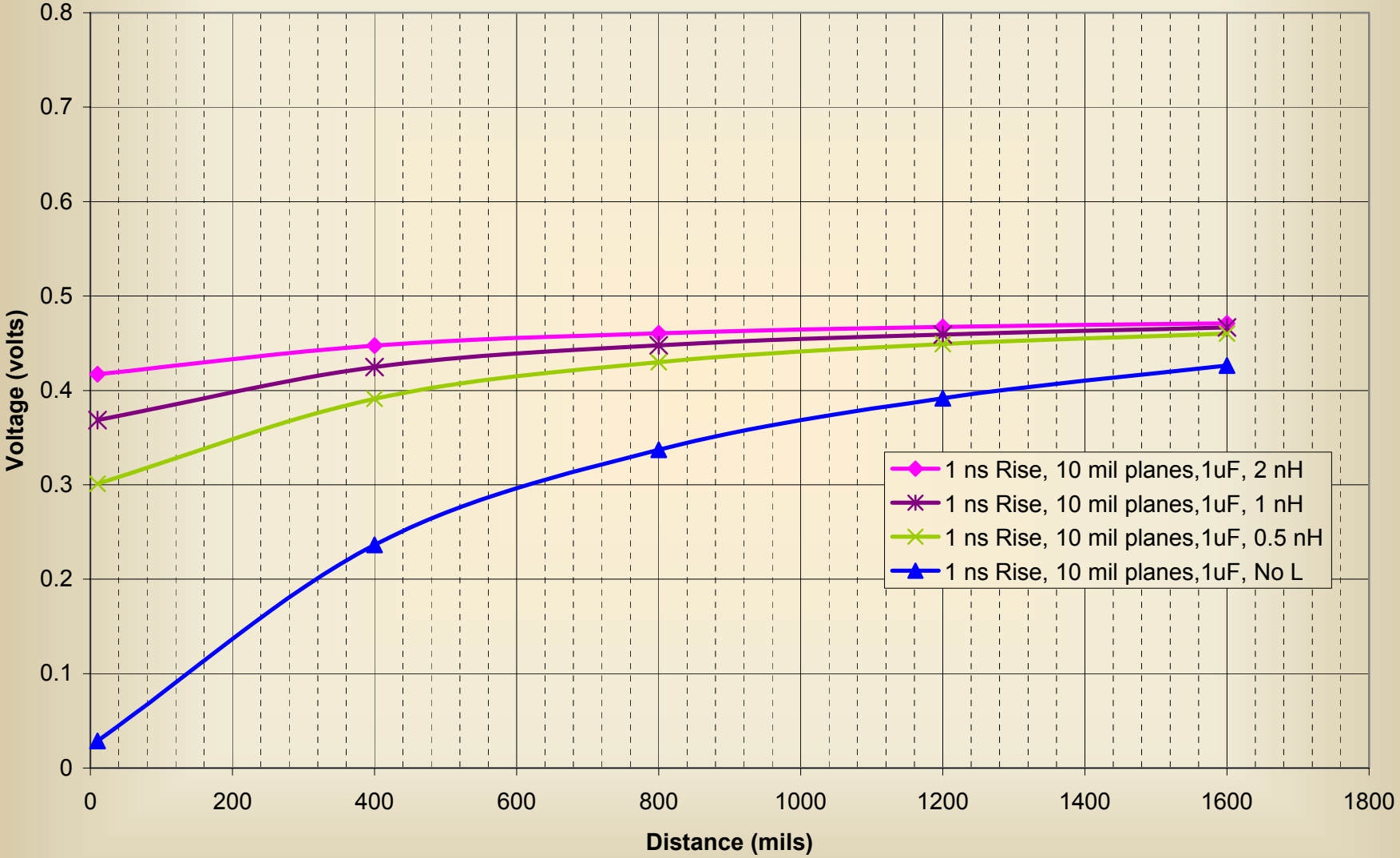
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor with Various Capacitor Connection Inductance



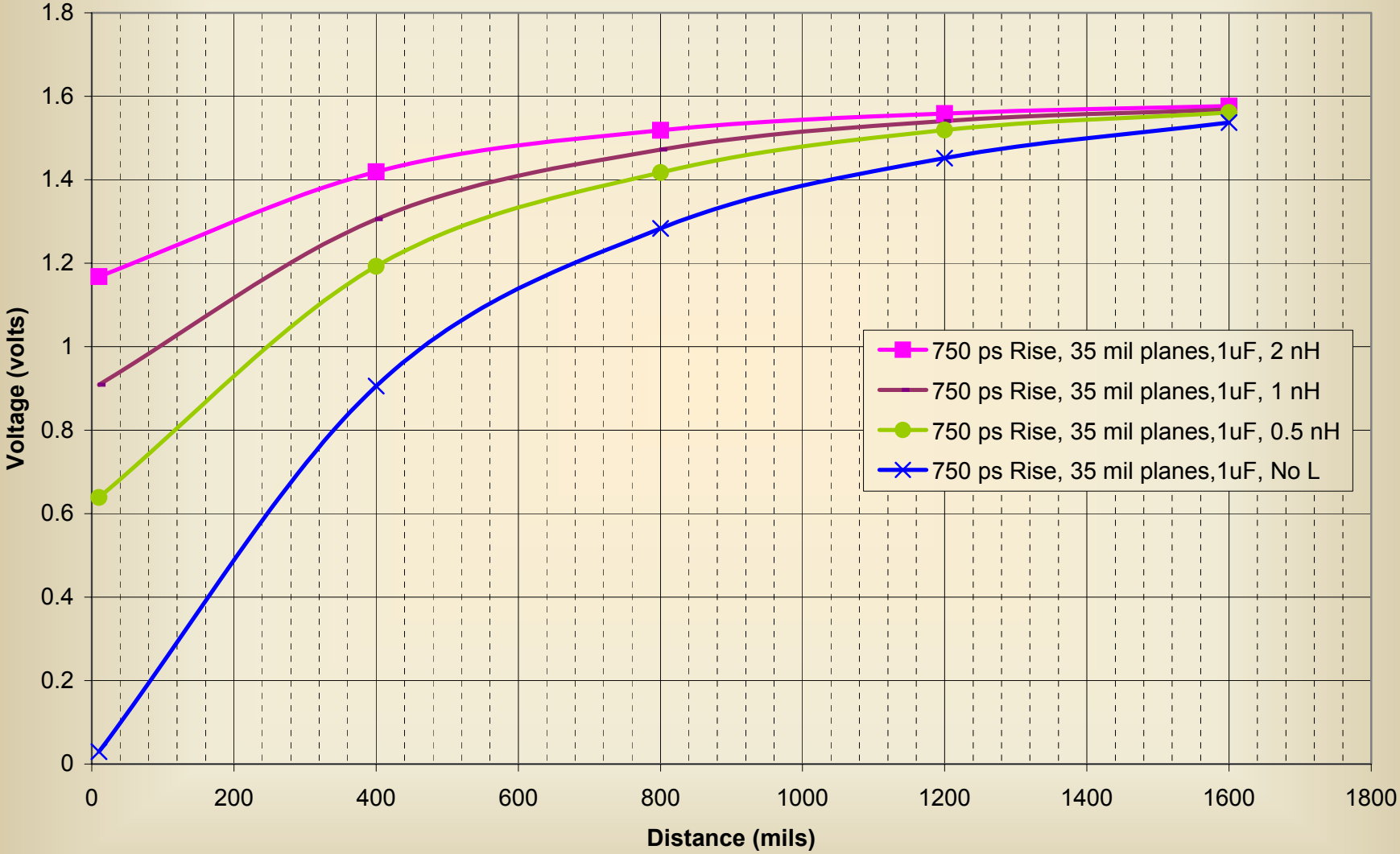
Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)



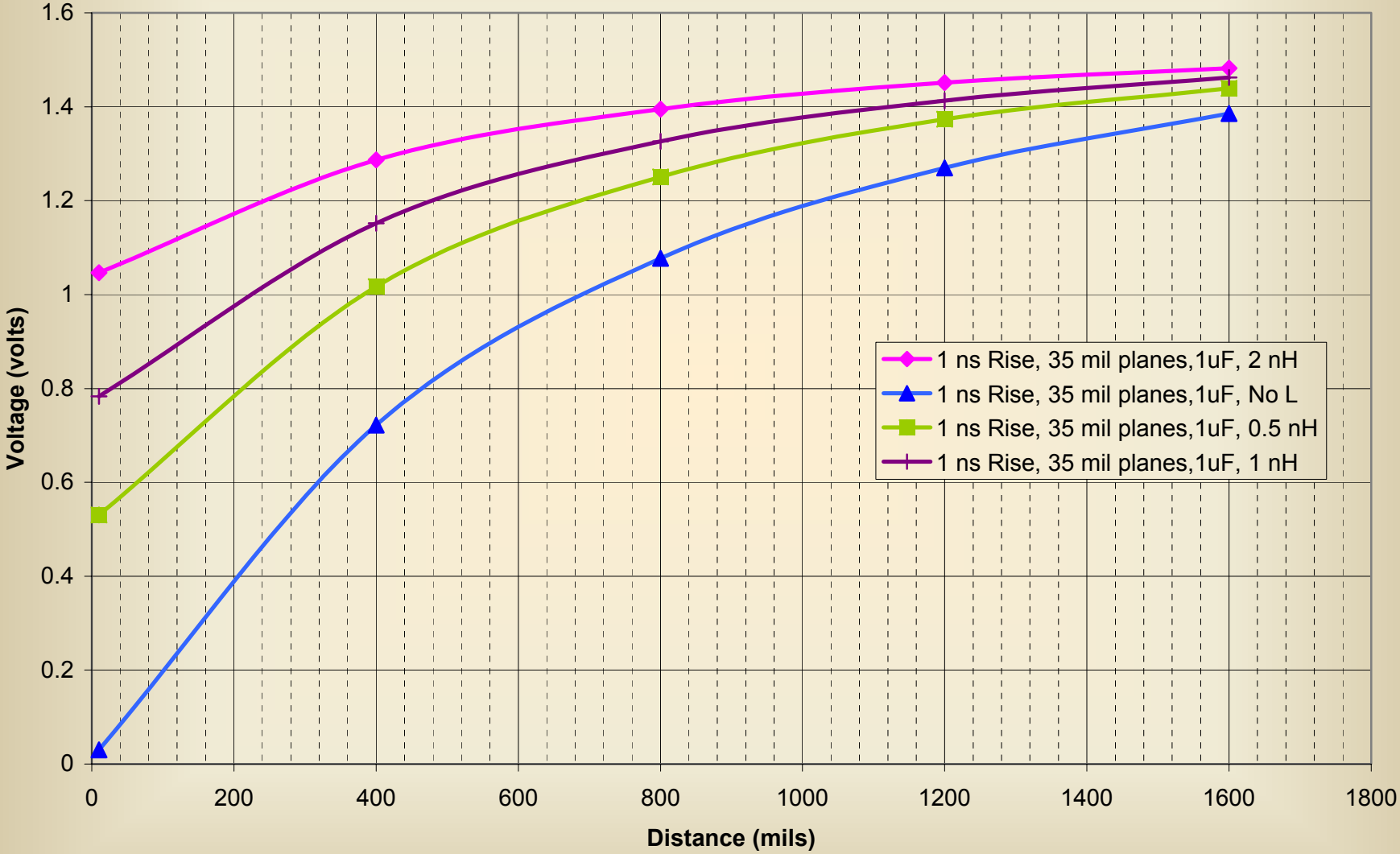
Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)

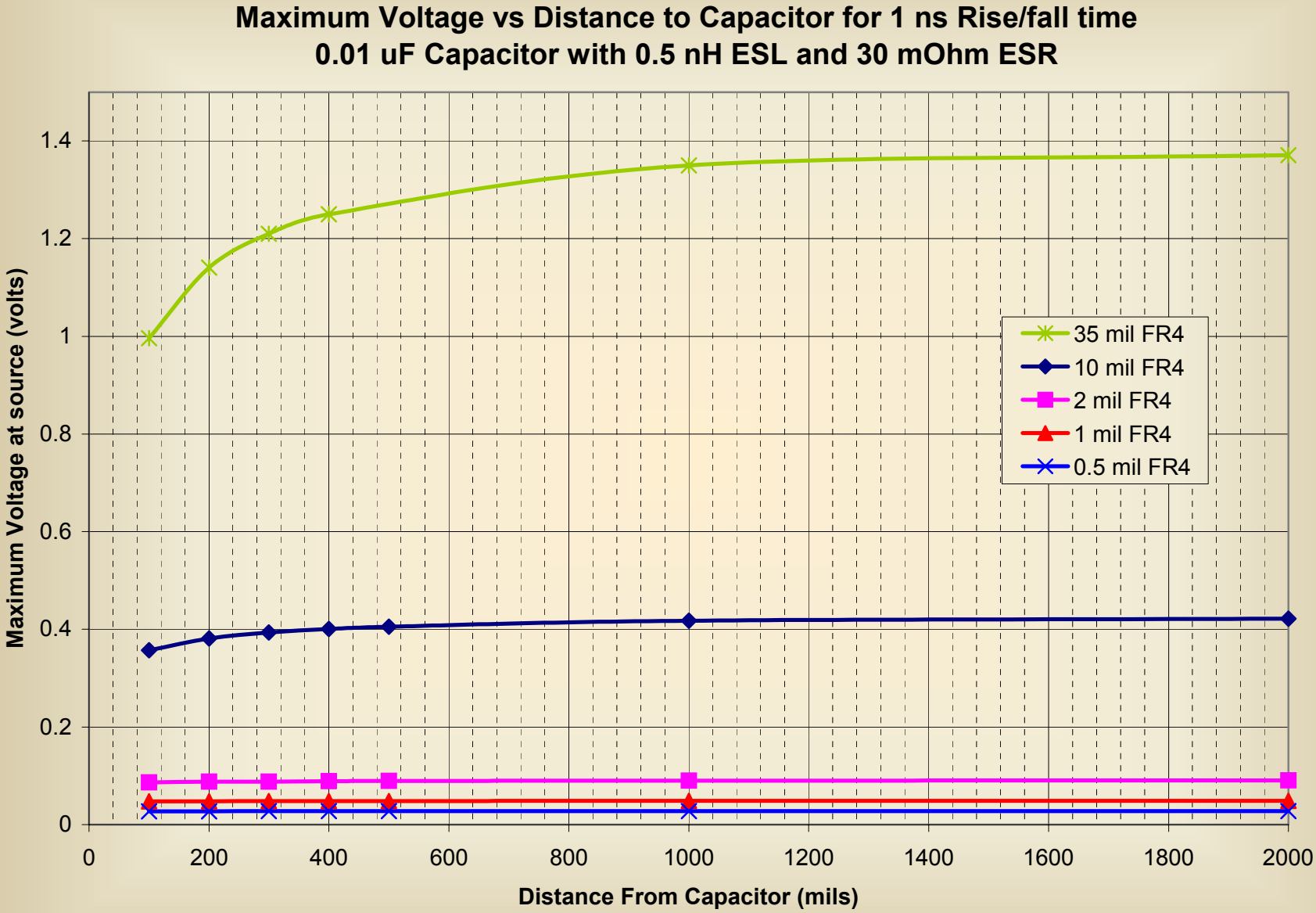


Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)



Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)




Maximum Voltage vs Distance to Capacitor for 1 ns Rise/fall time
0.01 uF Capacitor with 0.5 nH ESL and 30 mOhm ESR
Maximum Voltage at source (volts)
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
200
400
600
800
1000
1200
1400
1600
1800
2000
Distance From Capacitor (mils)
35 mil FR4
10 mil FR4
2 mil FR4
1 mil FR4
0.5 mil FR4

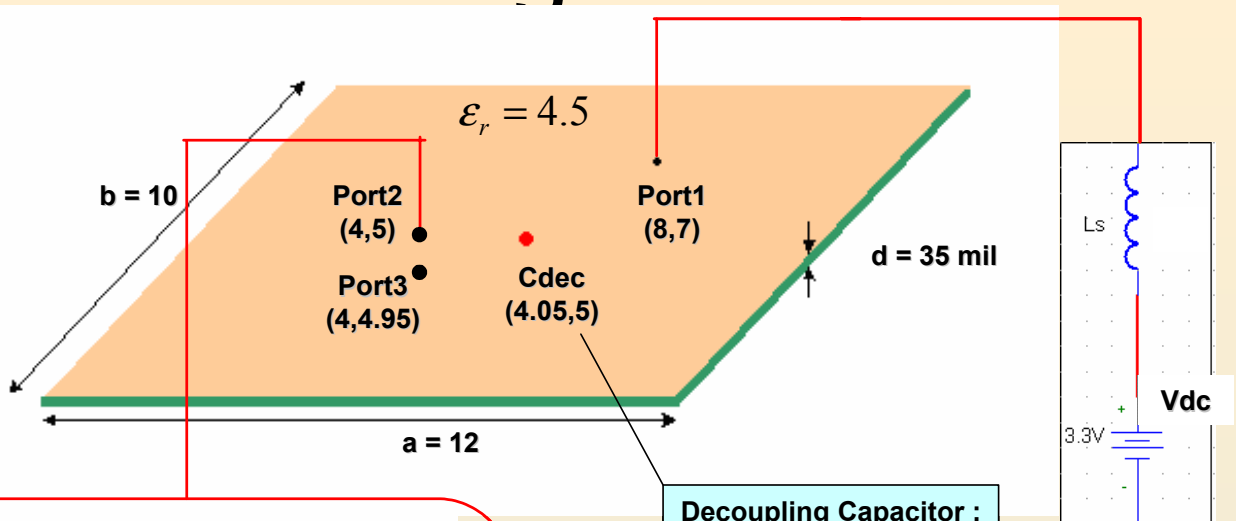
So Far……

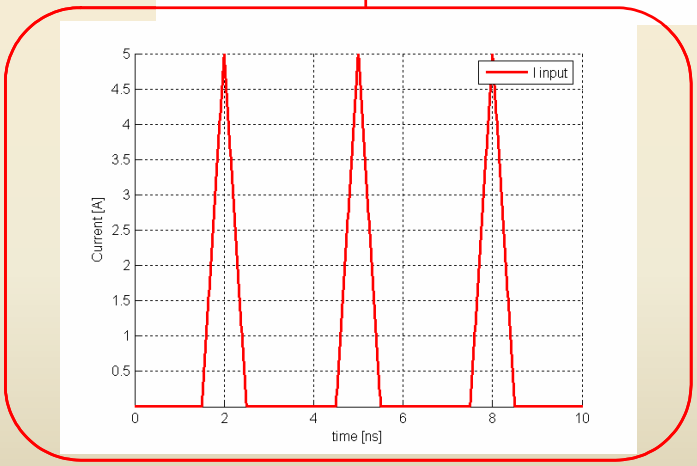
- Frequency domain simulations not optimum for charge delivery decoupling calculations (phase not considered)
- Time domain simulations using single pulse of current indicate limited capacitor location effect
  - Connection inductance of capacitor much higher than inductance between planes
  - Charge delivered only from the planes

Charge Depletion

- IC draws charge from planes
- Capacitors will re-charge planes
  - Location ***does*** matter!

Model for Plane Recharge Investigations





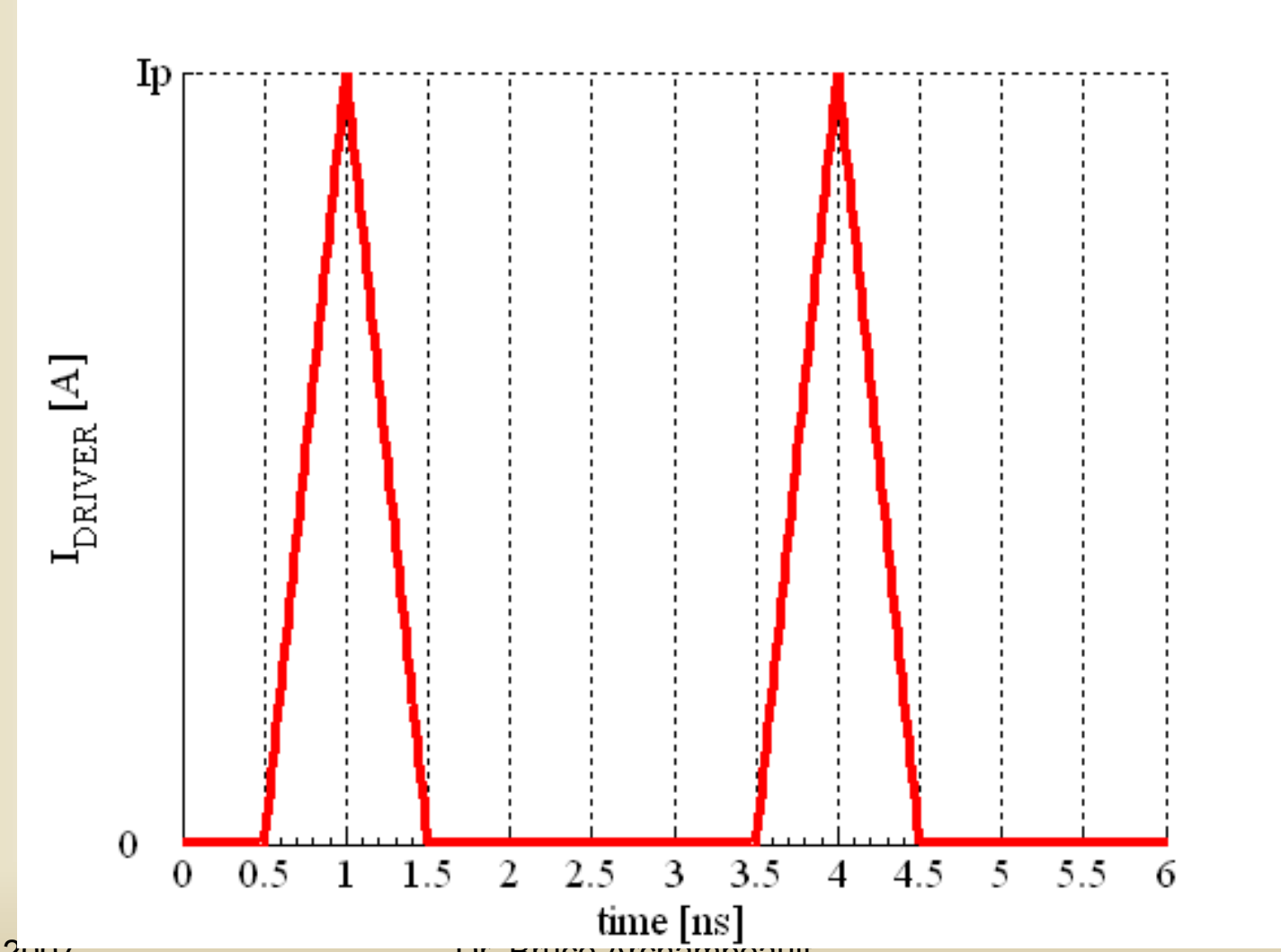
Port 2 represents IC current draw

Charge Between Planes vs.. Charge Drawn by IC

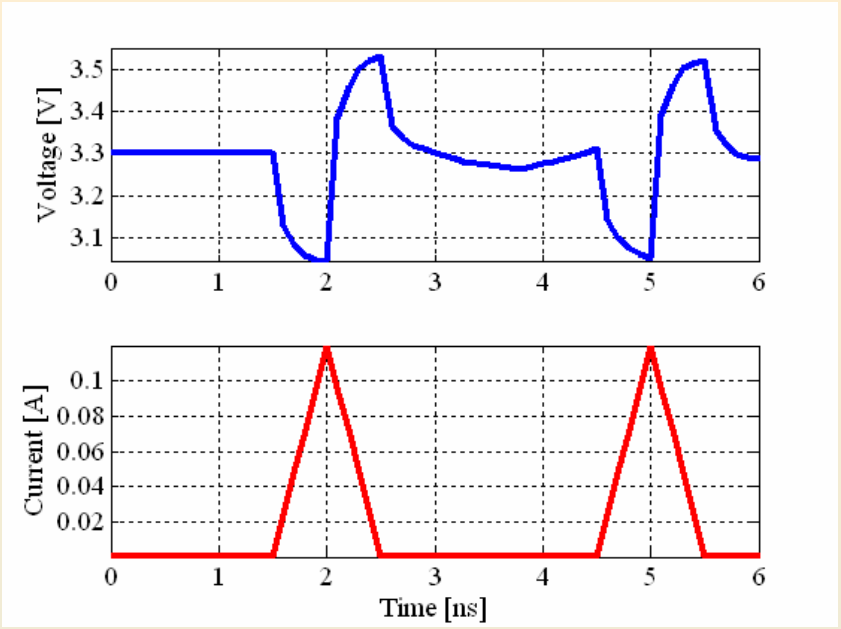
Board total charge : C*V = 3.5nF*3.3V = 11nC

Pulse charge 5A peak : I*dt/2 = (1ns*5A)/2=2.5nC

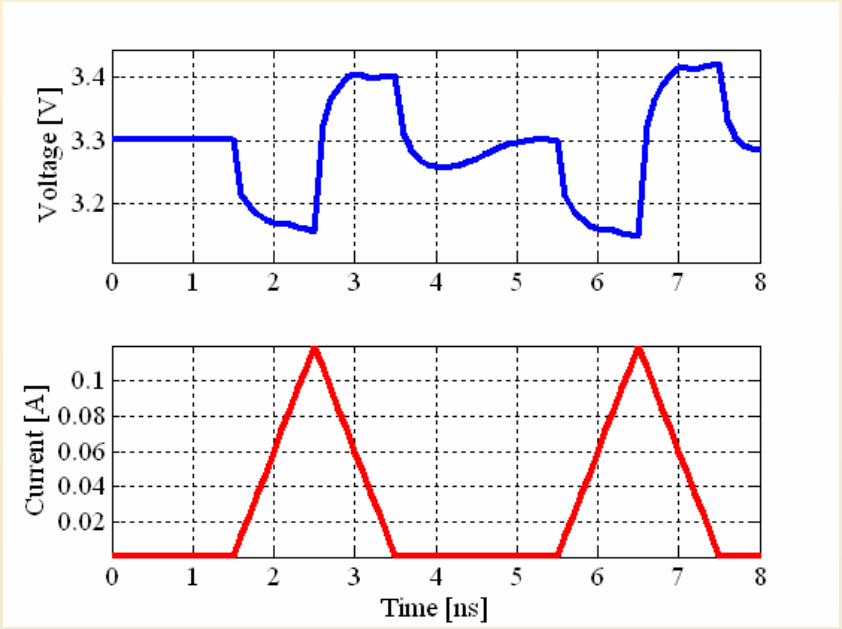
Triangular pulses (5 Amps Peak)



Noise Voltage from Inductive Effect of Current Draw



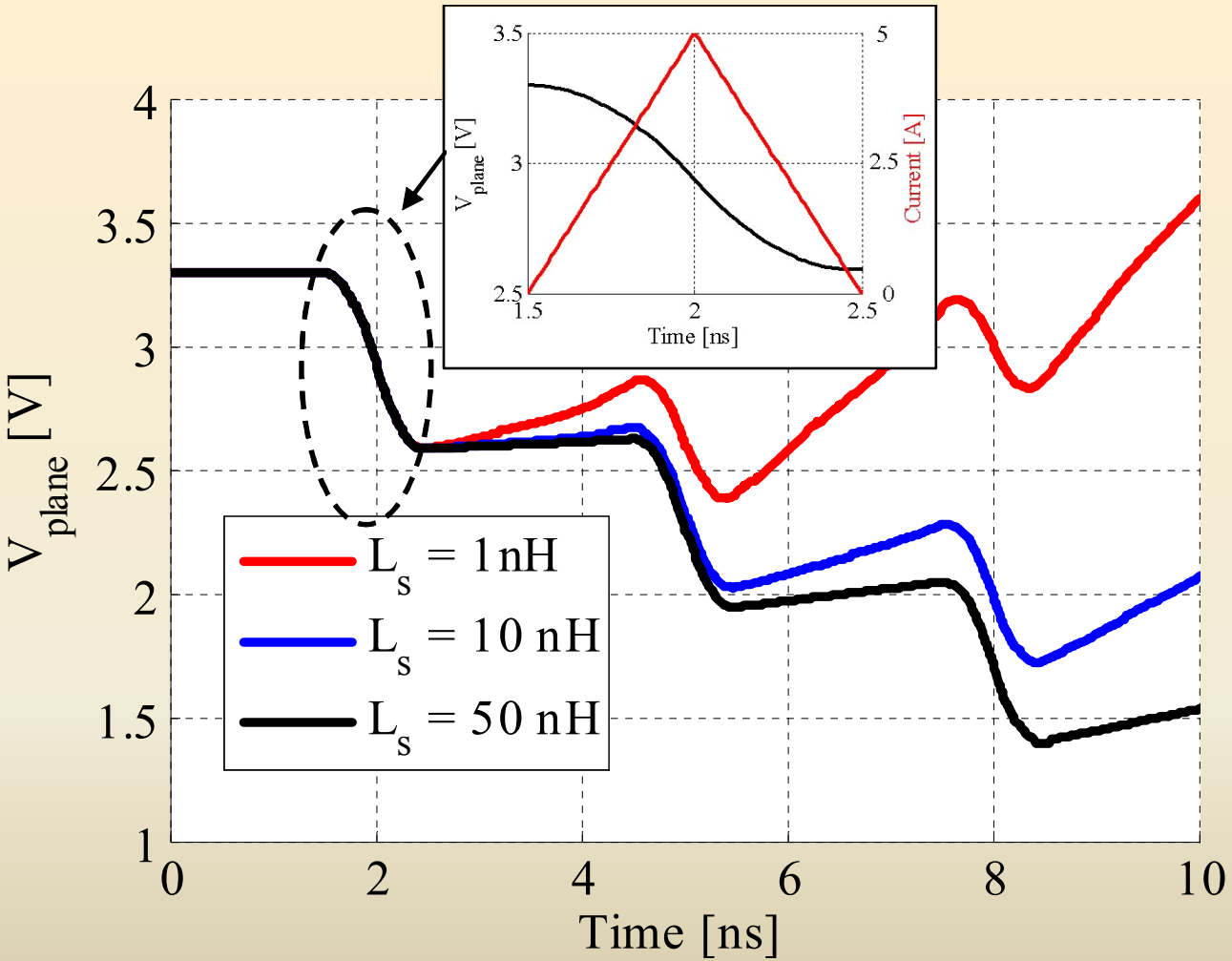
(a)



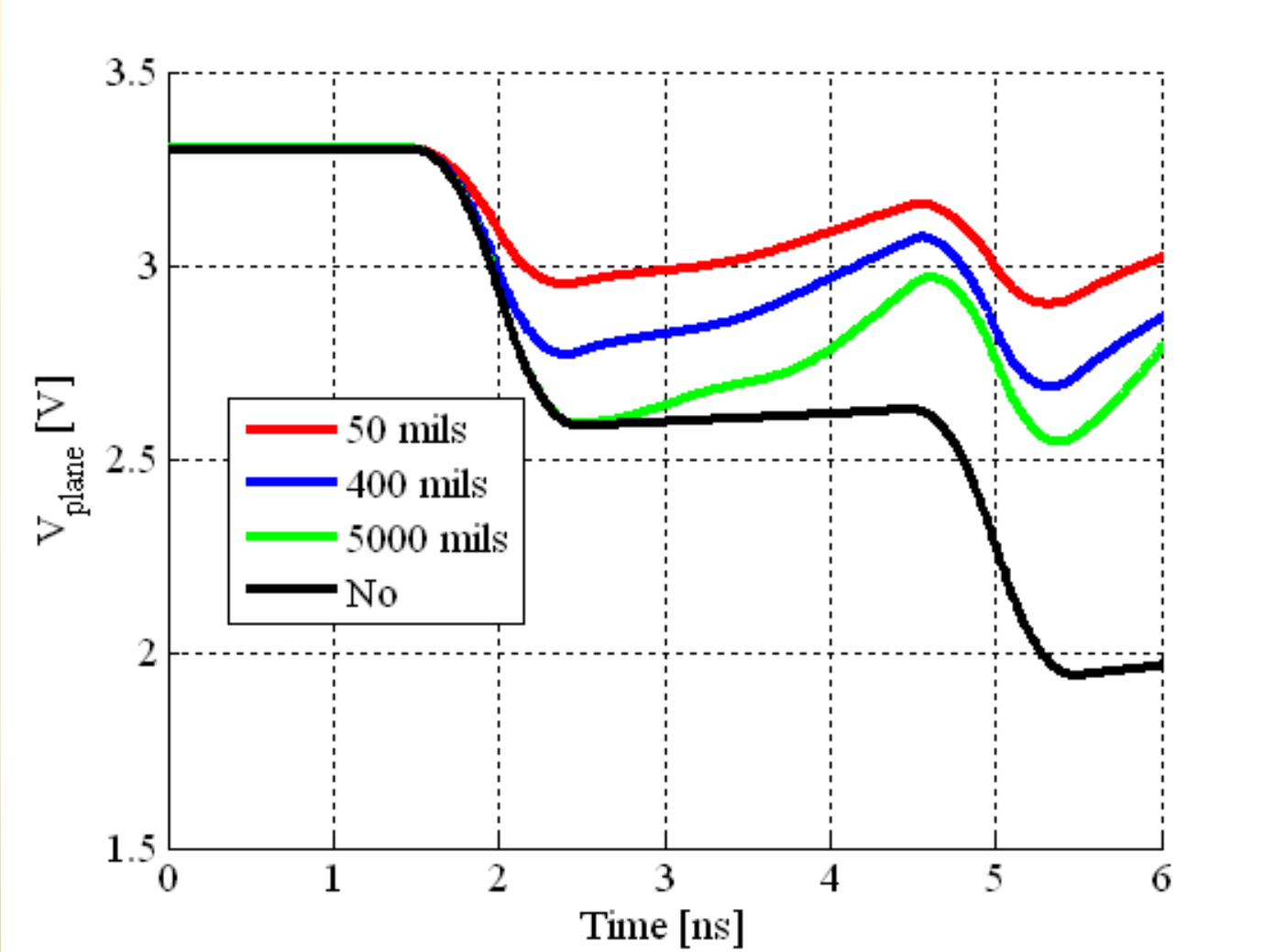
(b)

Current pulses too small to see charge depletion effects in this time scale

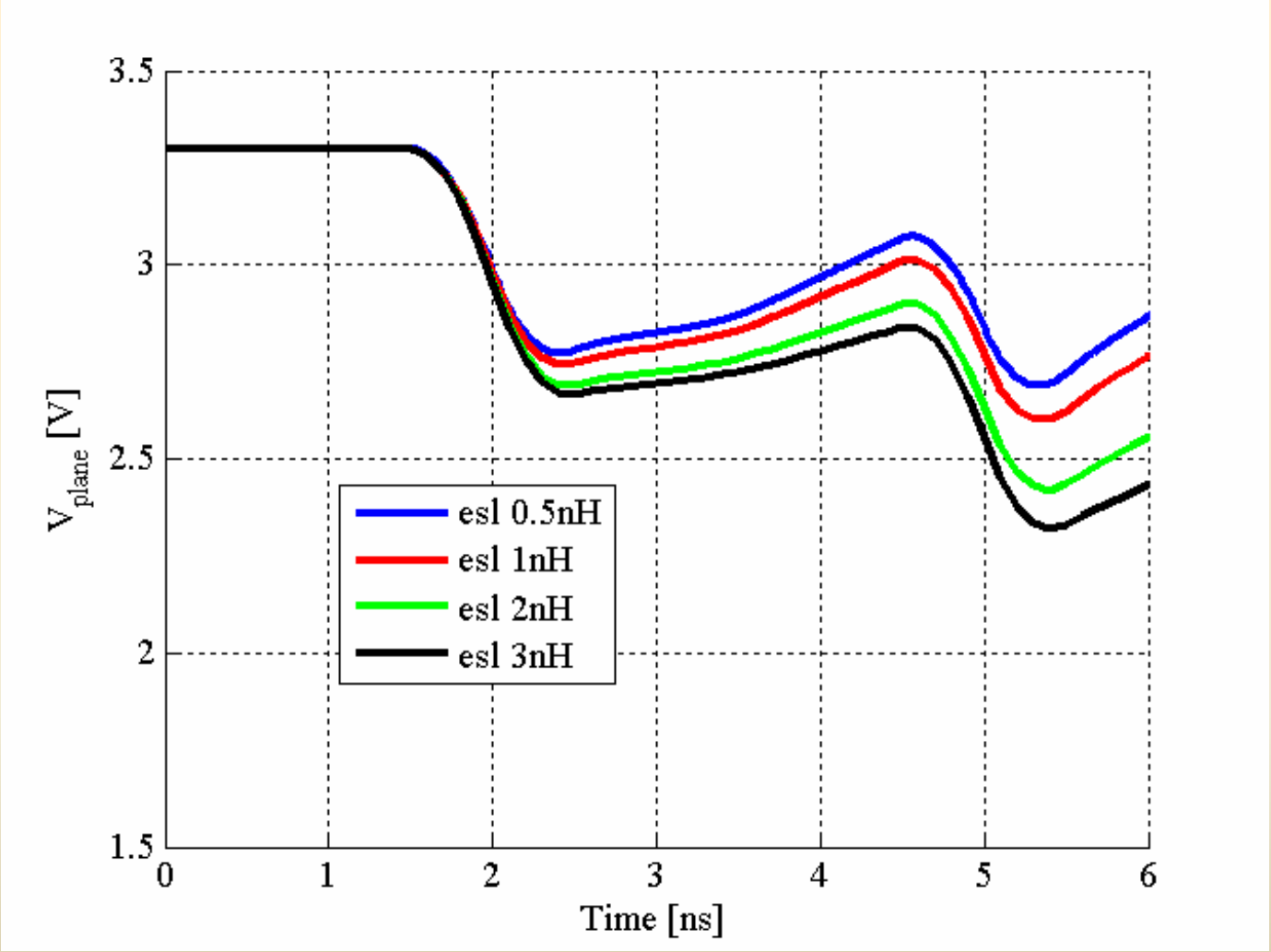
Charge Depletion → Voltage Drop



Charge Depletion vs. Capacitor Distance



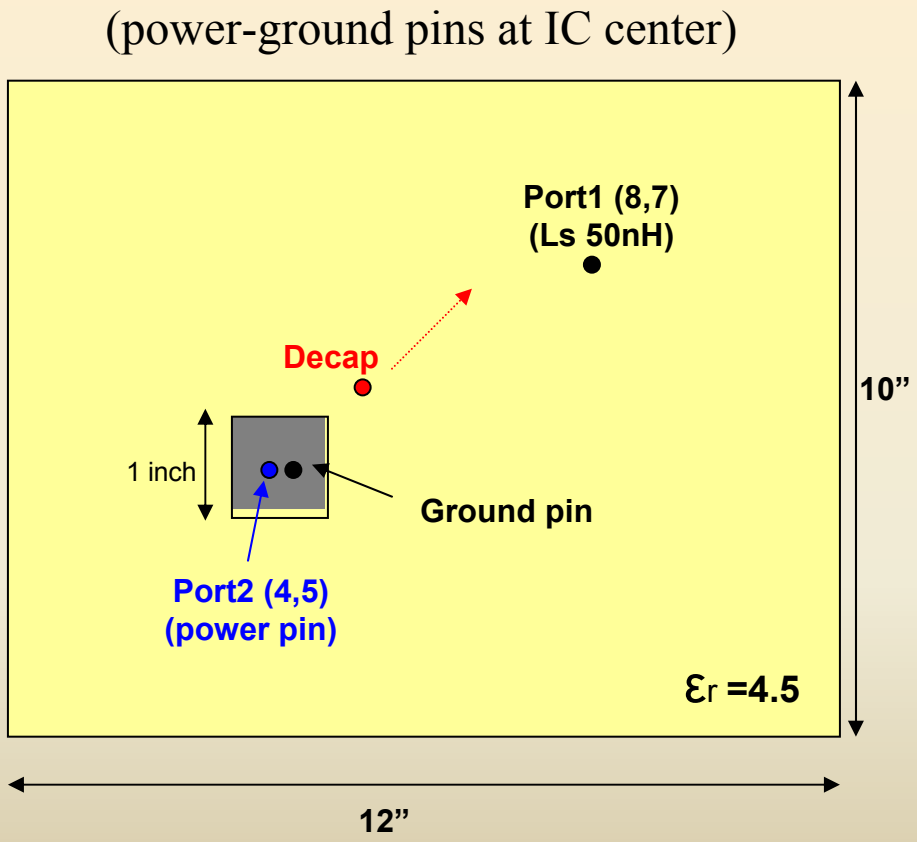
Charge Depletion for Capacitor @ 400 mils for Various Connection Inductance



Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils, 1200mils, 2700mils from the power pin

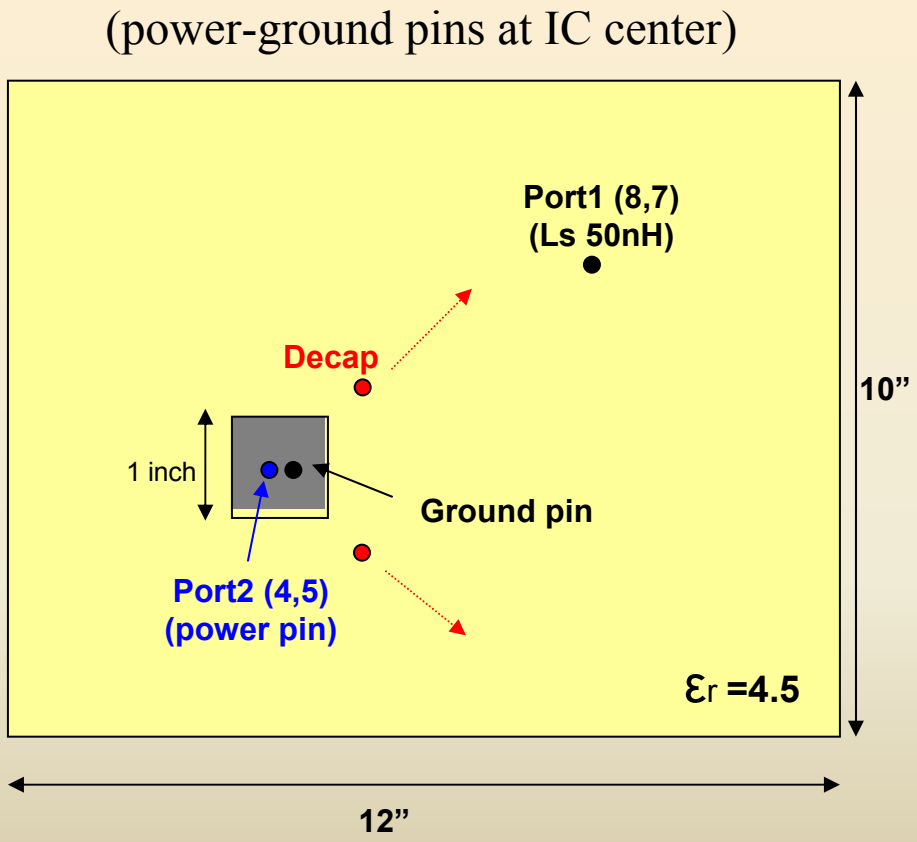
- C=1uF
- ESL=0.5nH
- ESR=1Ω



Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils, 1200mils, 2700mils from the power pin

- C=0.5uF
- ESL=0.5nH
- ESR=1Ω

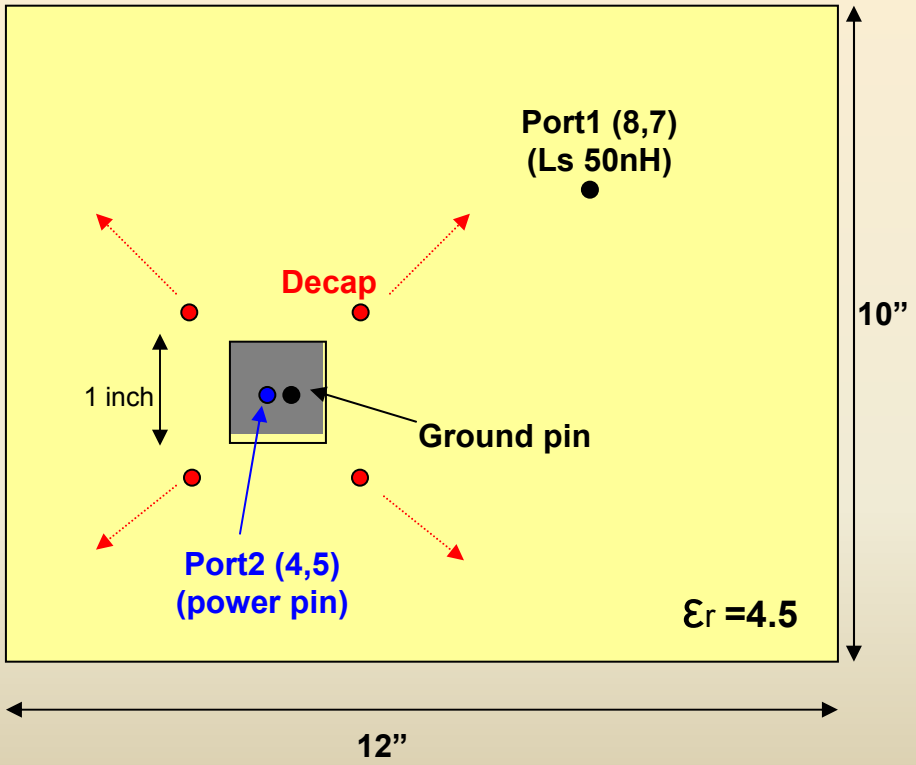


Effect of Multiple Capacitors While Keeping Total Capacitance Constant

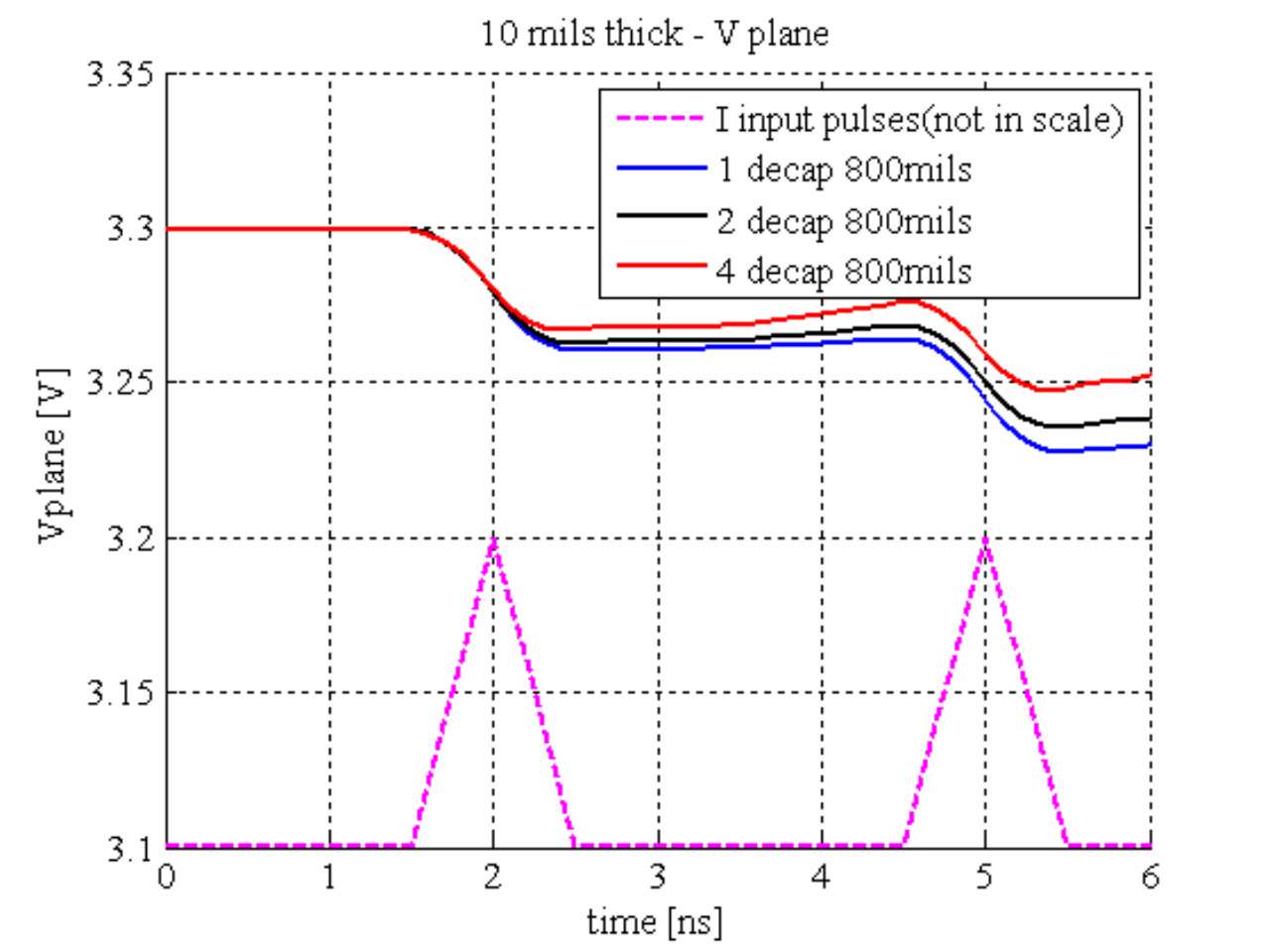
The decap locations are 800mils, 1200mils, 2700mils from the power pin

- C=0.25uF
- ESL=0.5nH
- ESR=1Ω

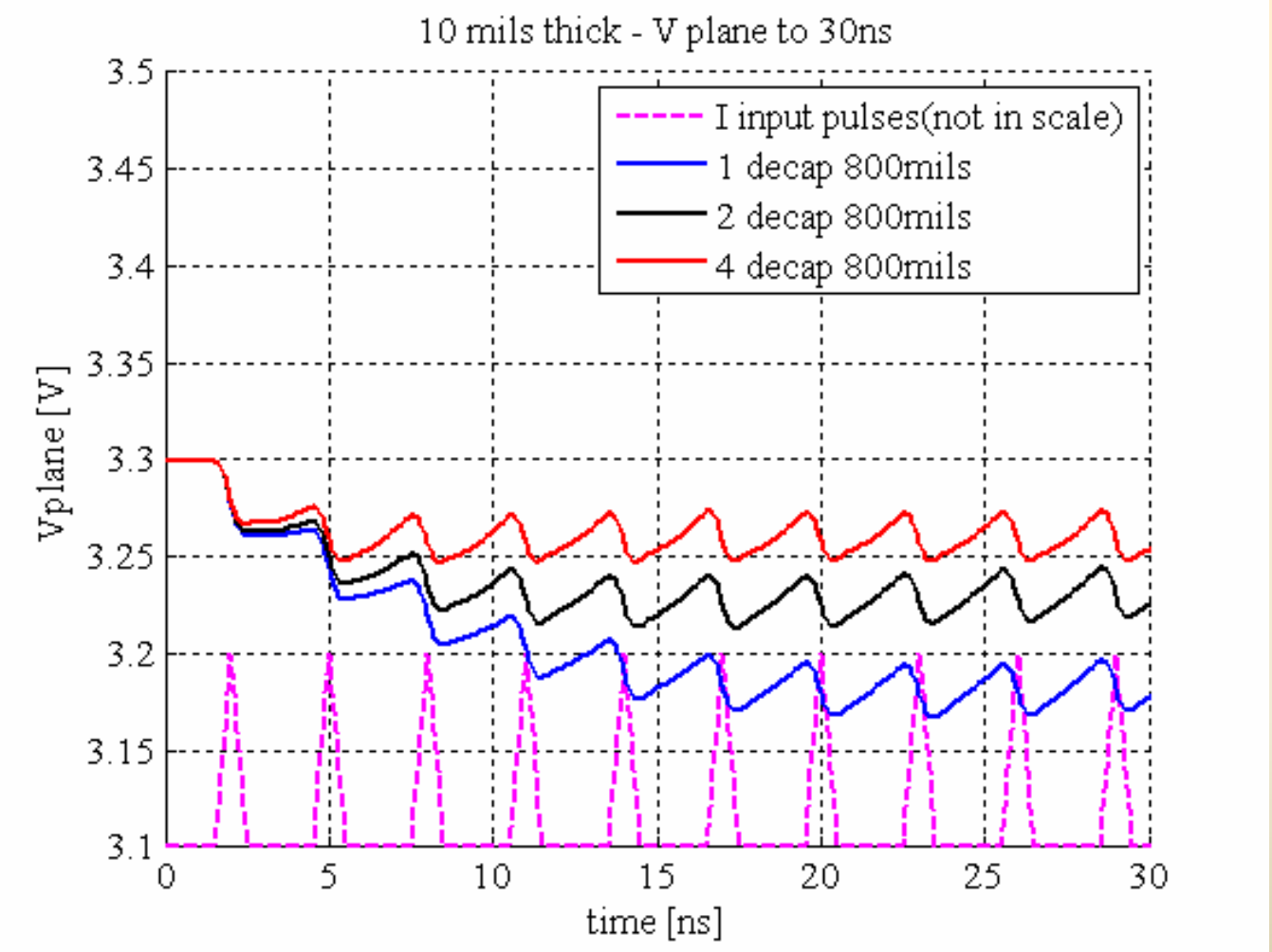
(power-ground pins at IC center)



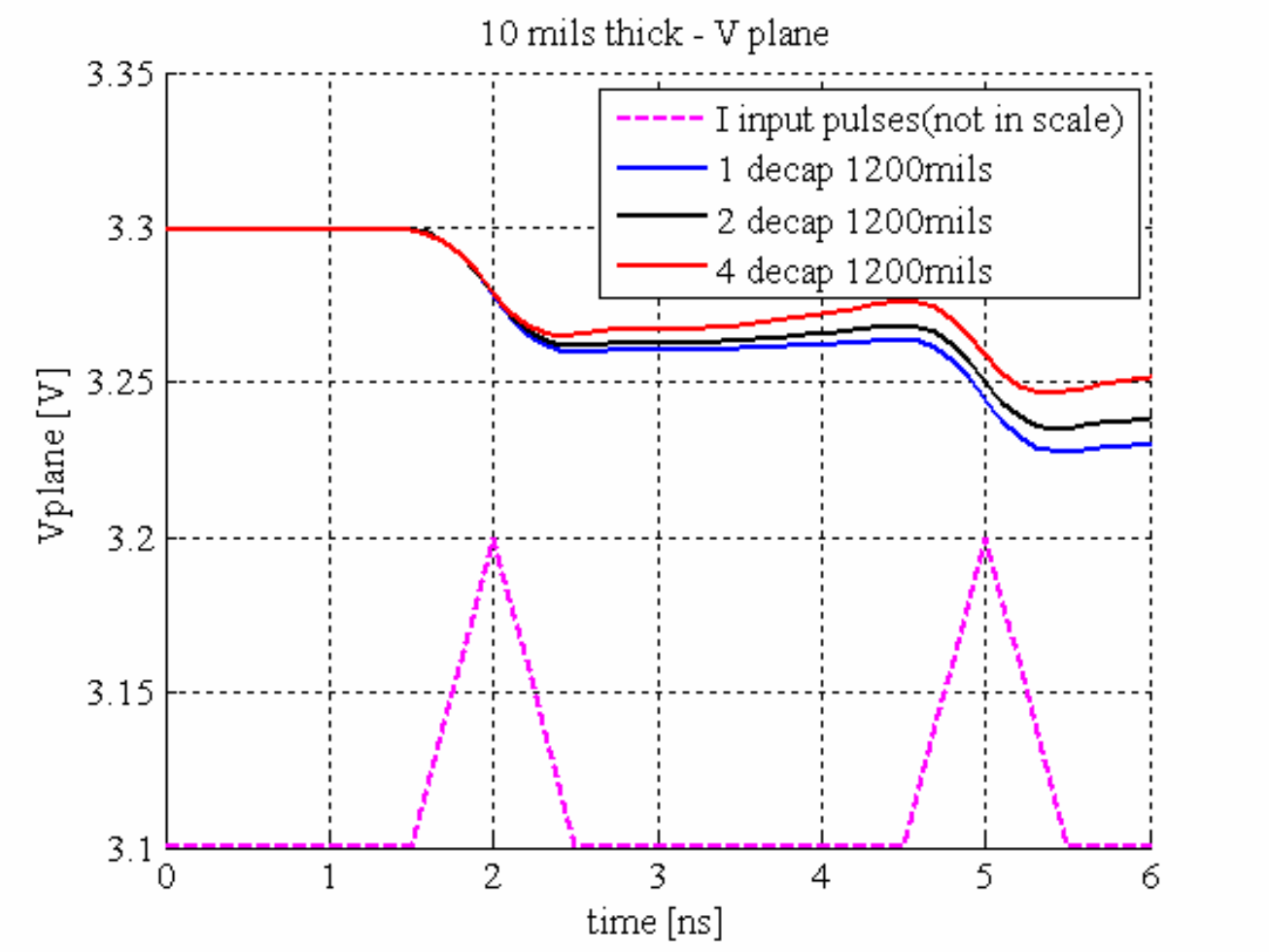
Constant Capacitance 800 mil Distance



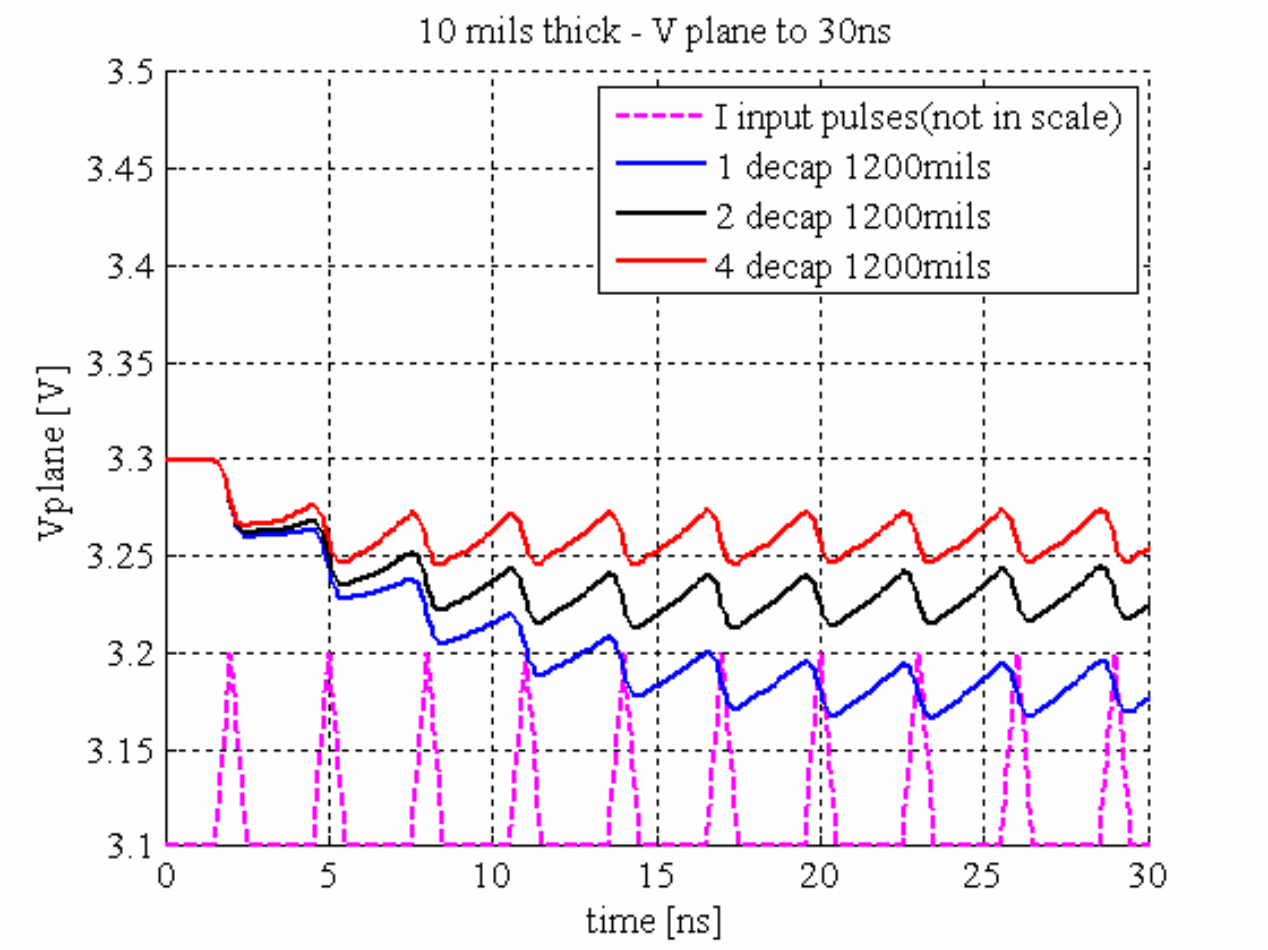
Constant Capacitance 800 mil Distance



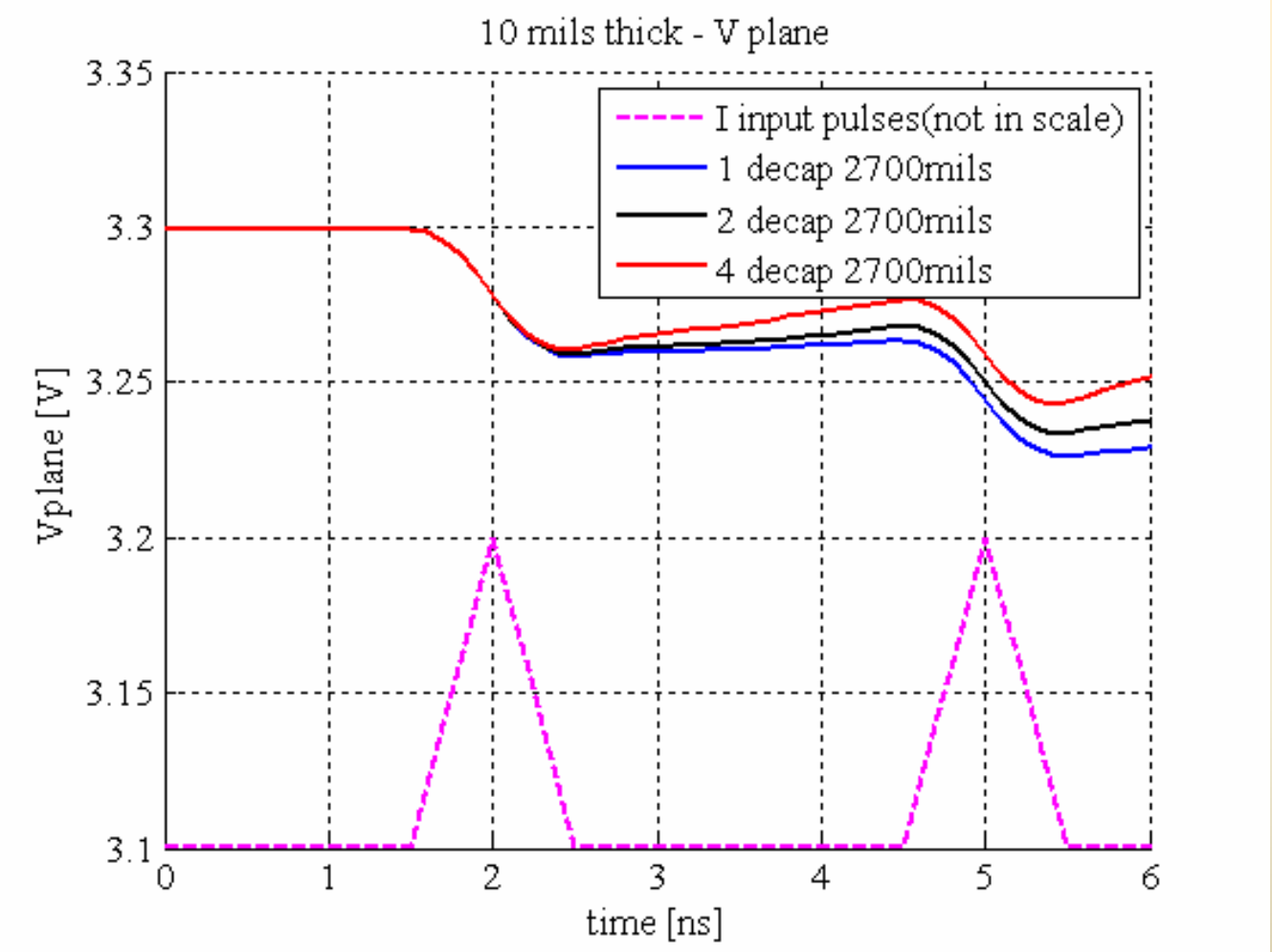
Constant Capacitance 1200 mil Distance



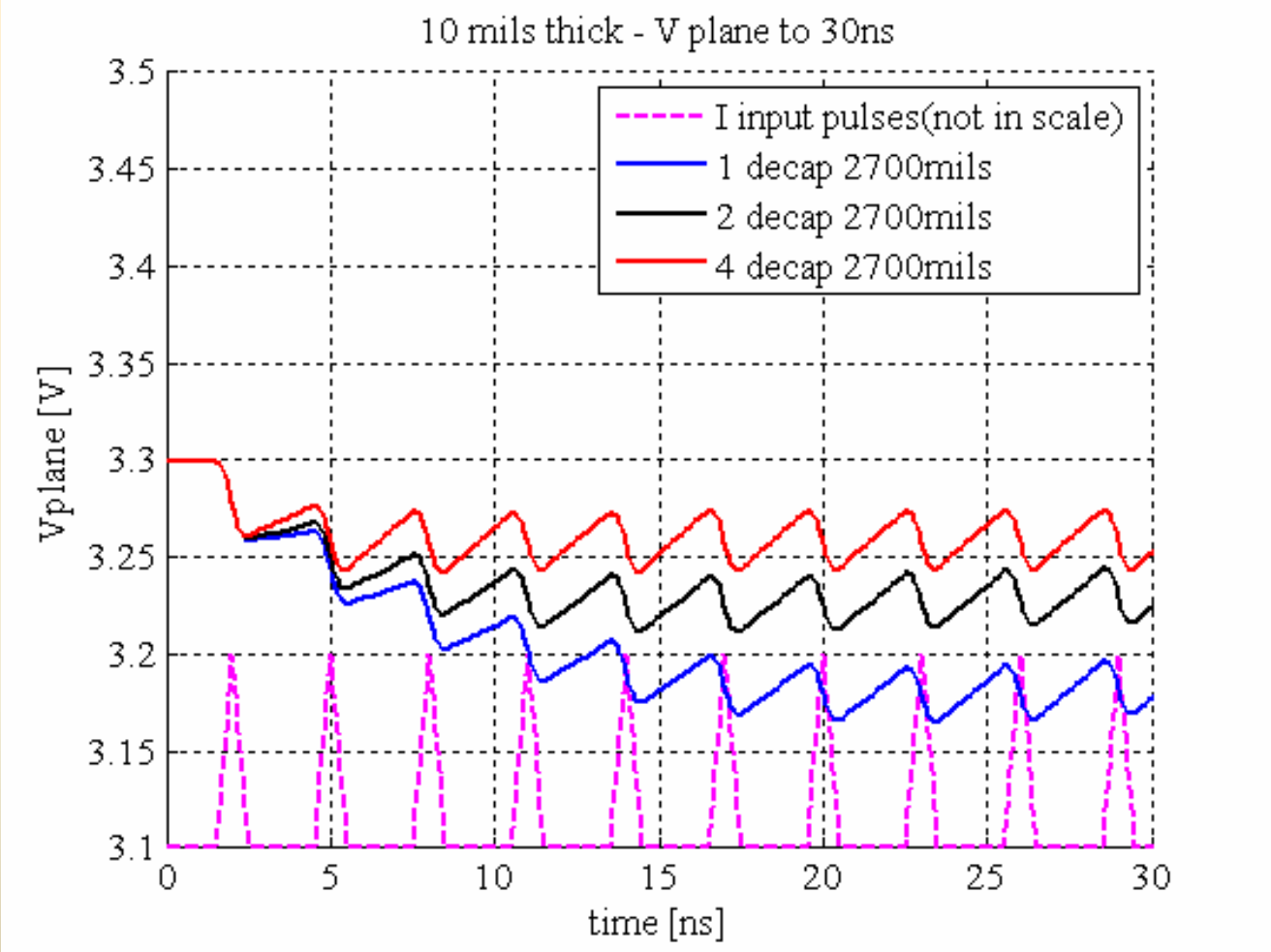
Constant Capacitance 1200 mil Distance



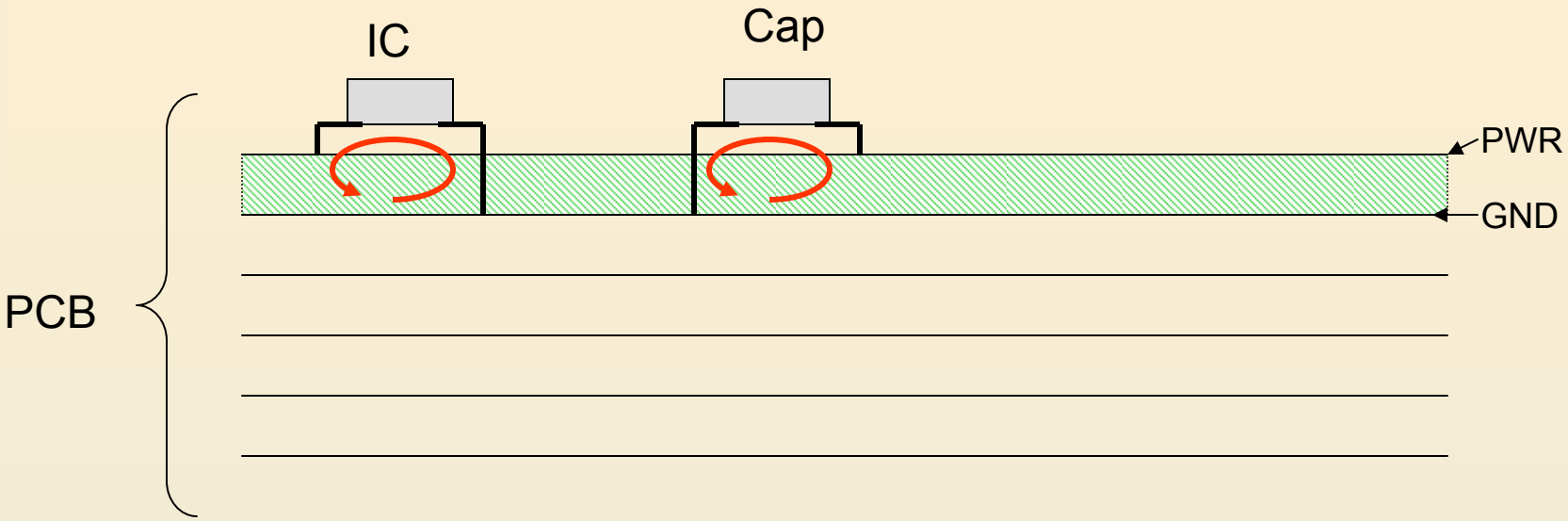
Constant Capacitance 2700 mil Distance



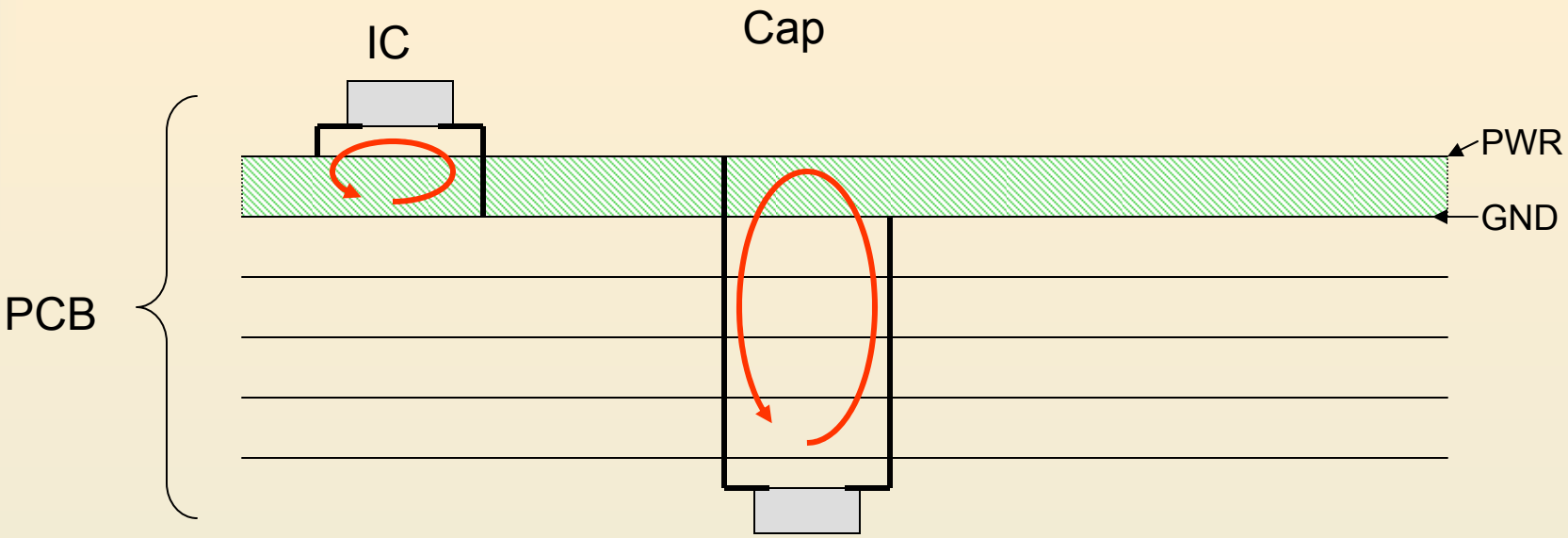
Constant Capacitance 2700 mil Distance



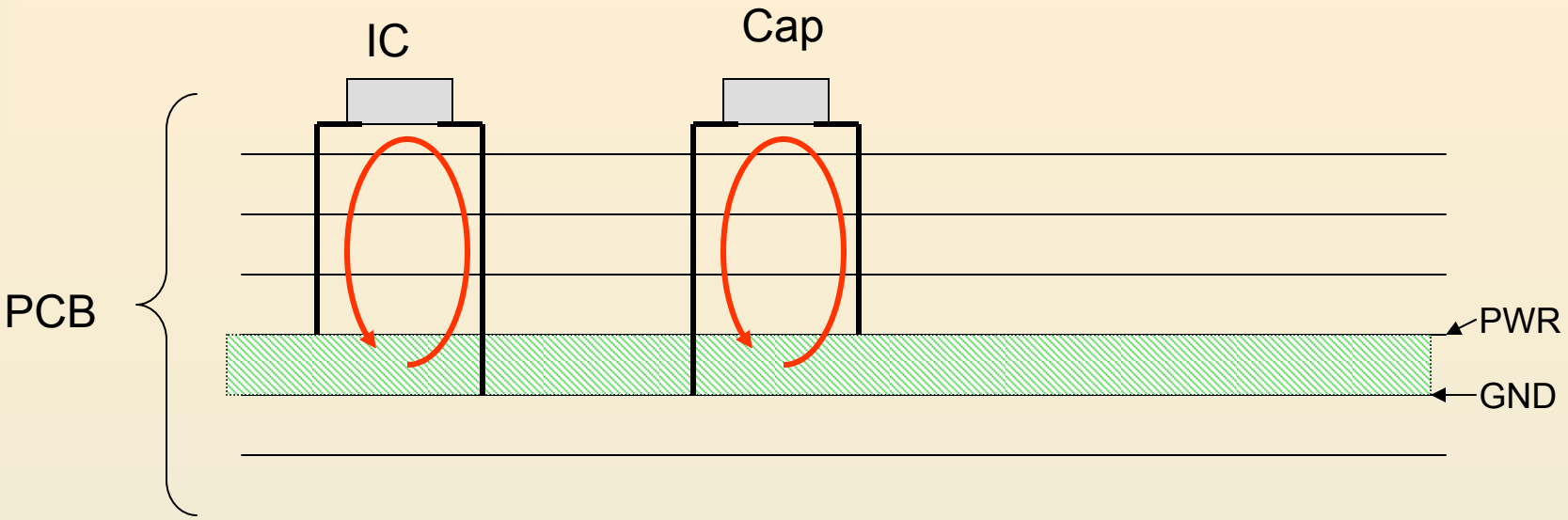
Example #1
Low Cap Connection Inductance



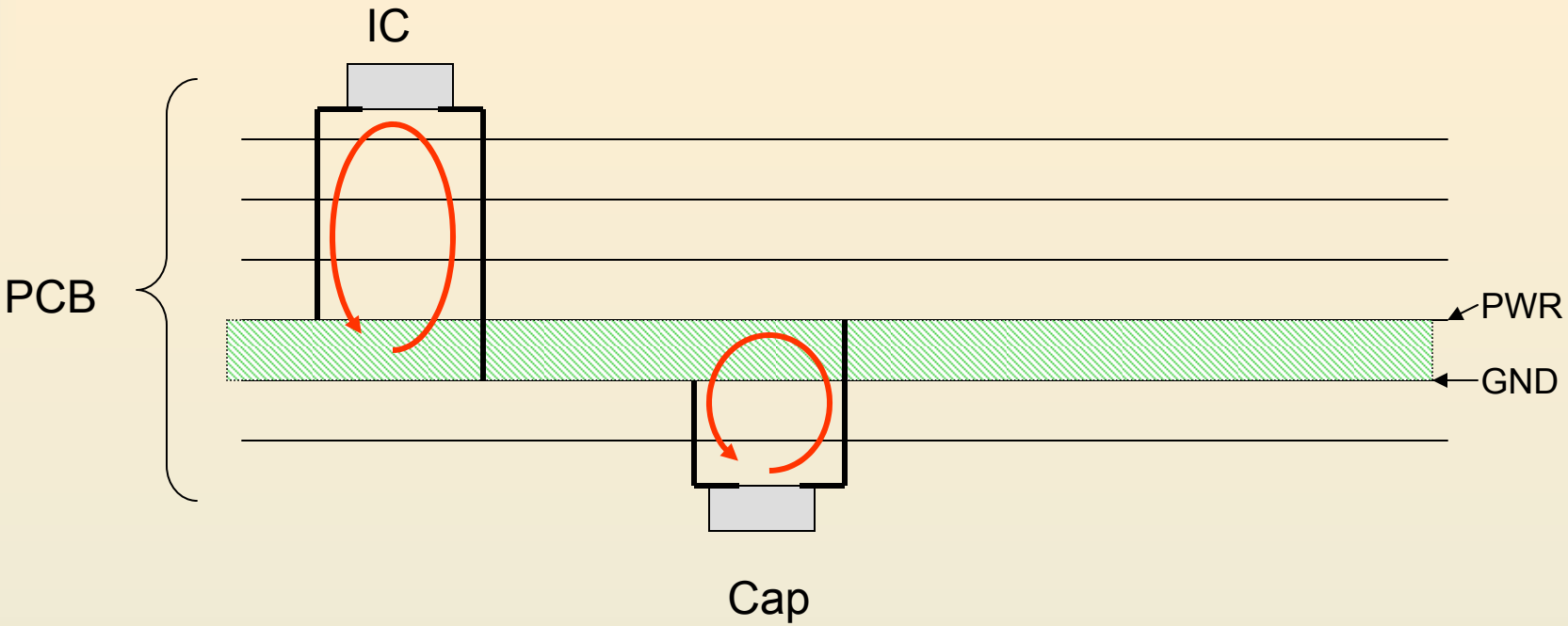
Example #2
High Cap Connection Inductance



Example #1
Hi Cap Connection Inductance



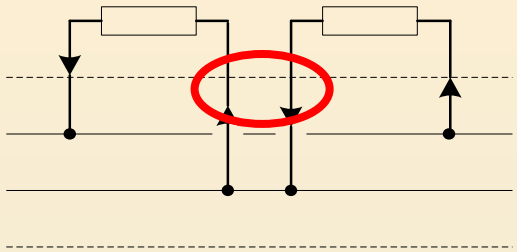
Example #1
Lower Cap Connection Inductance

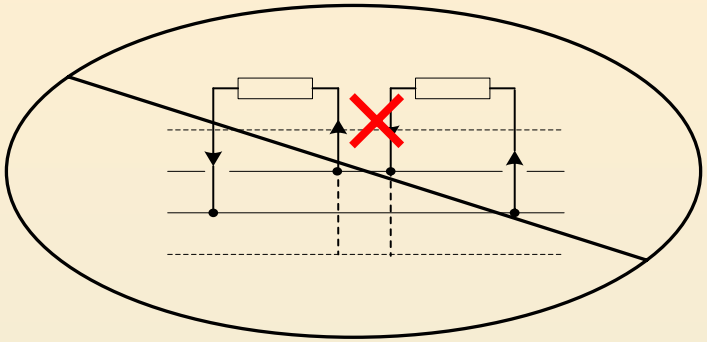


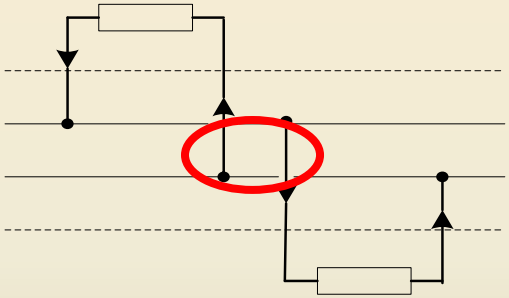
Mutual Inductance Helps Reduce Path Inductance

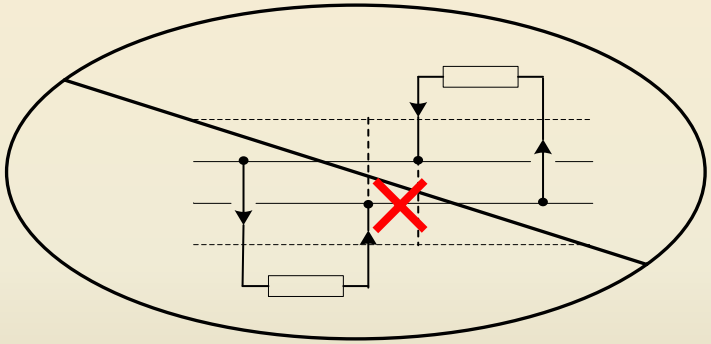
Do's

Don'ts









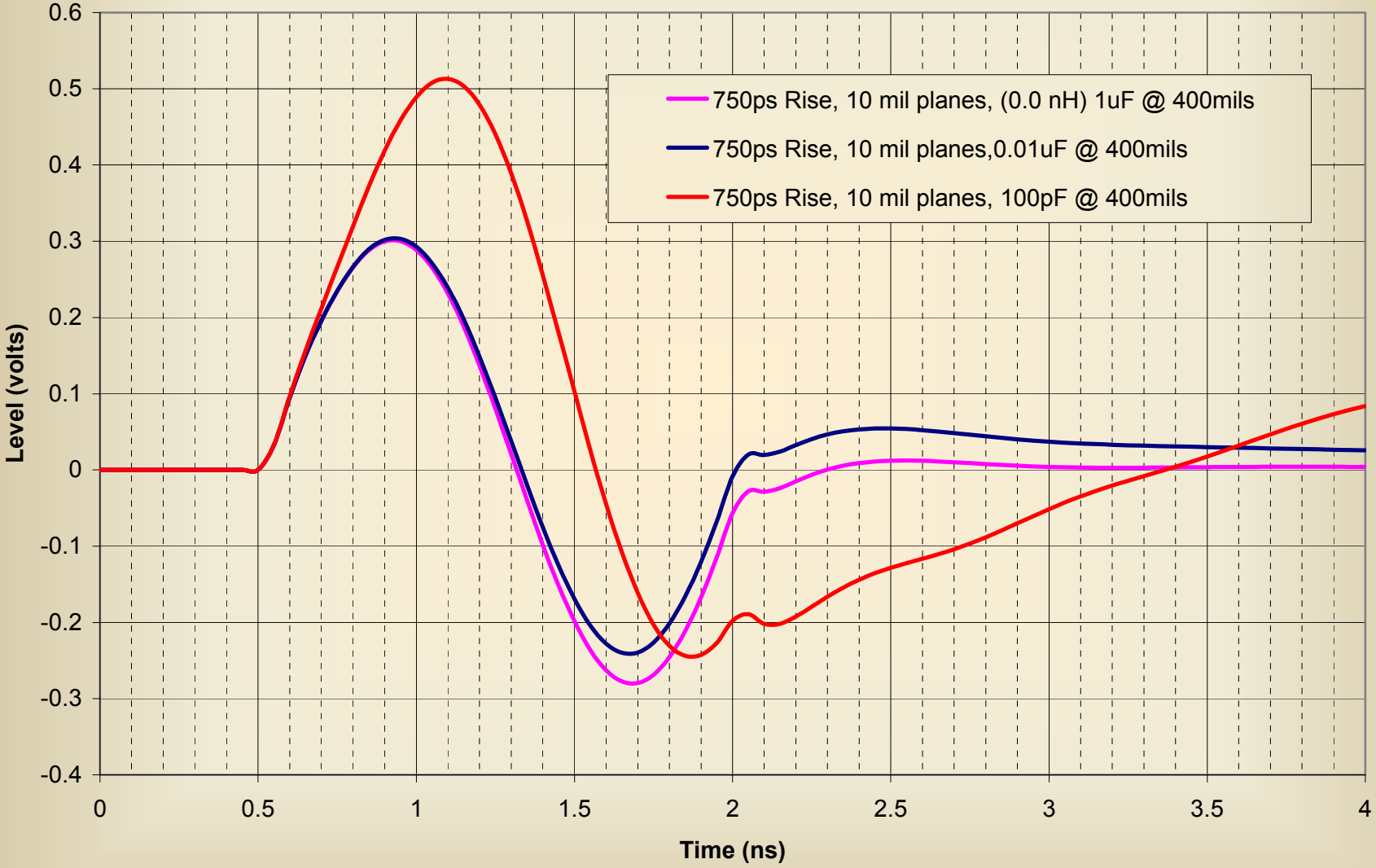
J. L Knighten, B. Archambeault, J. Fan, et. al., "PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?," *IEEE EMC Society Newsletter*, Issue No. 207, Winter 2006, pp. 56-67.

Effect of Capacitor Value??

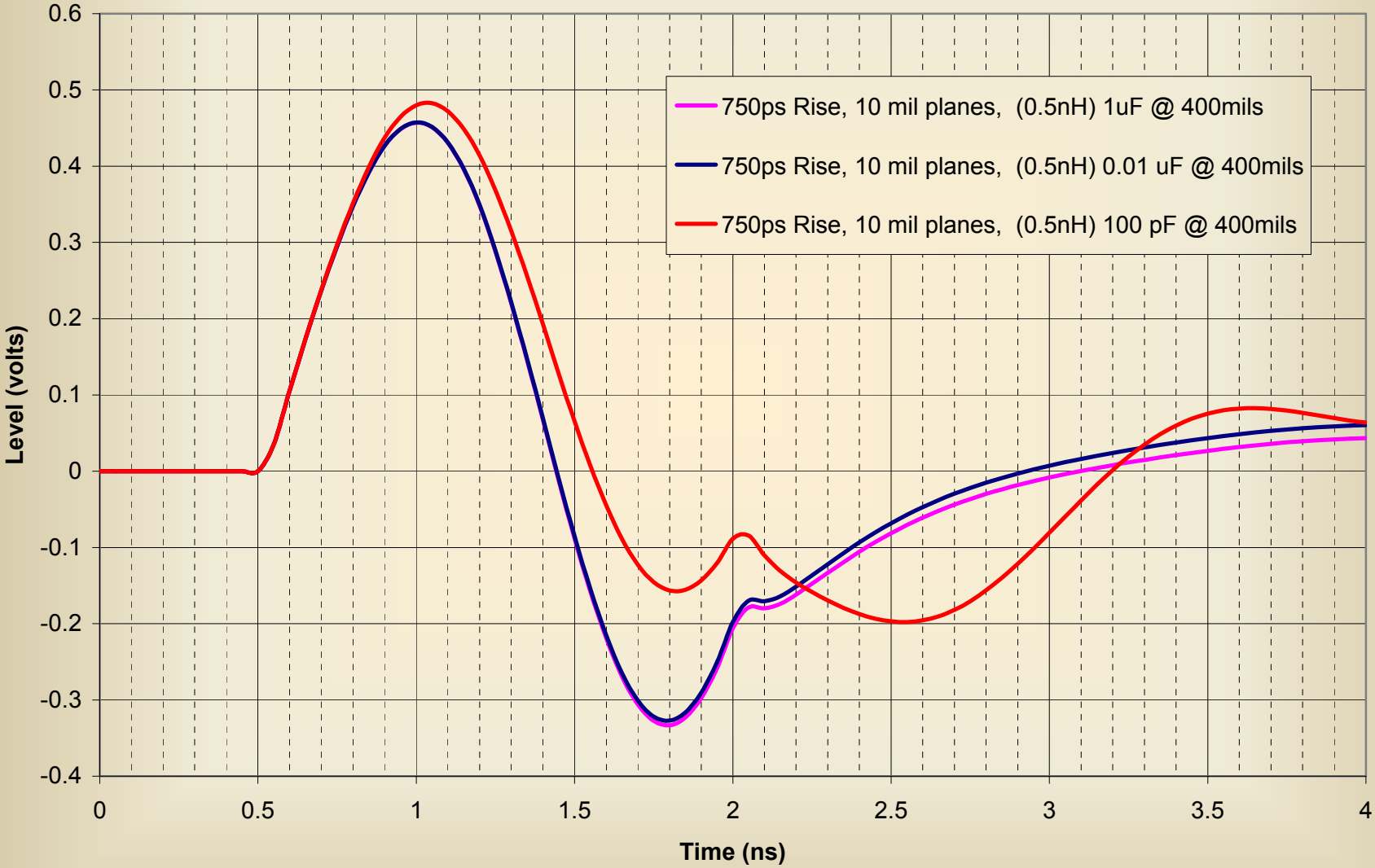
- Need enough charge to supply need
- Depends on connection inductance

Charge = C*V

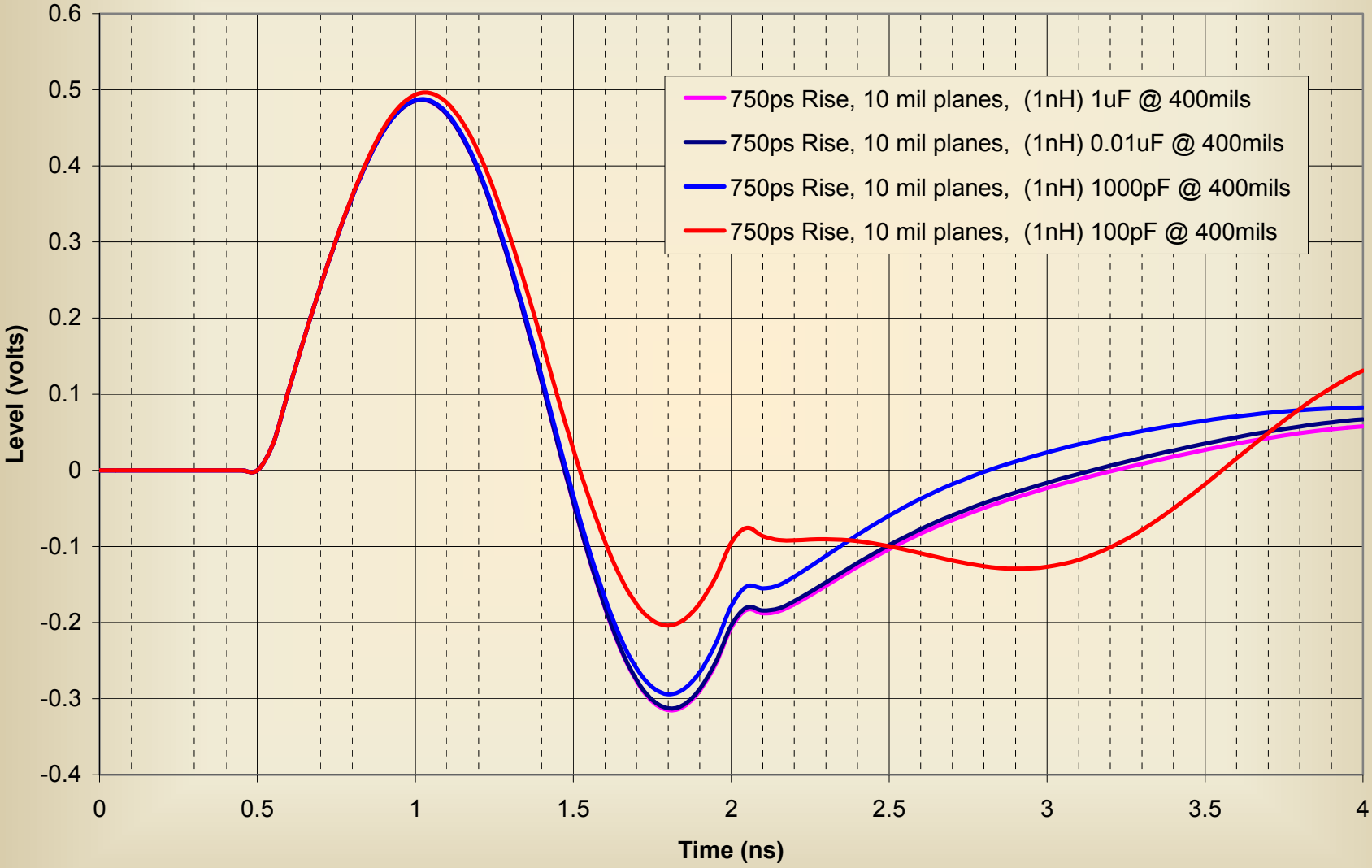
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with No L) with Various Capacitor Values



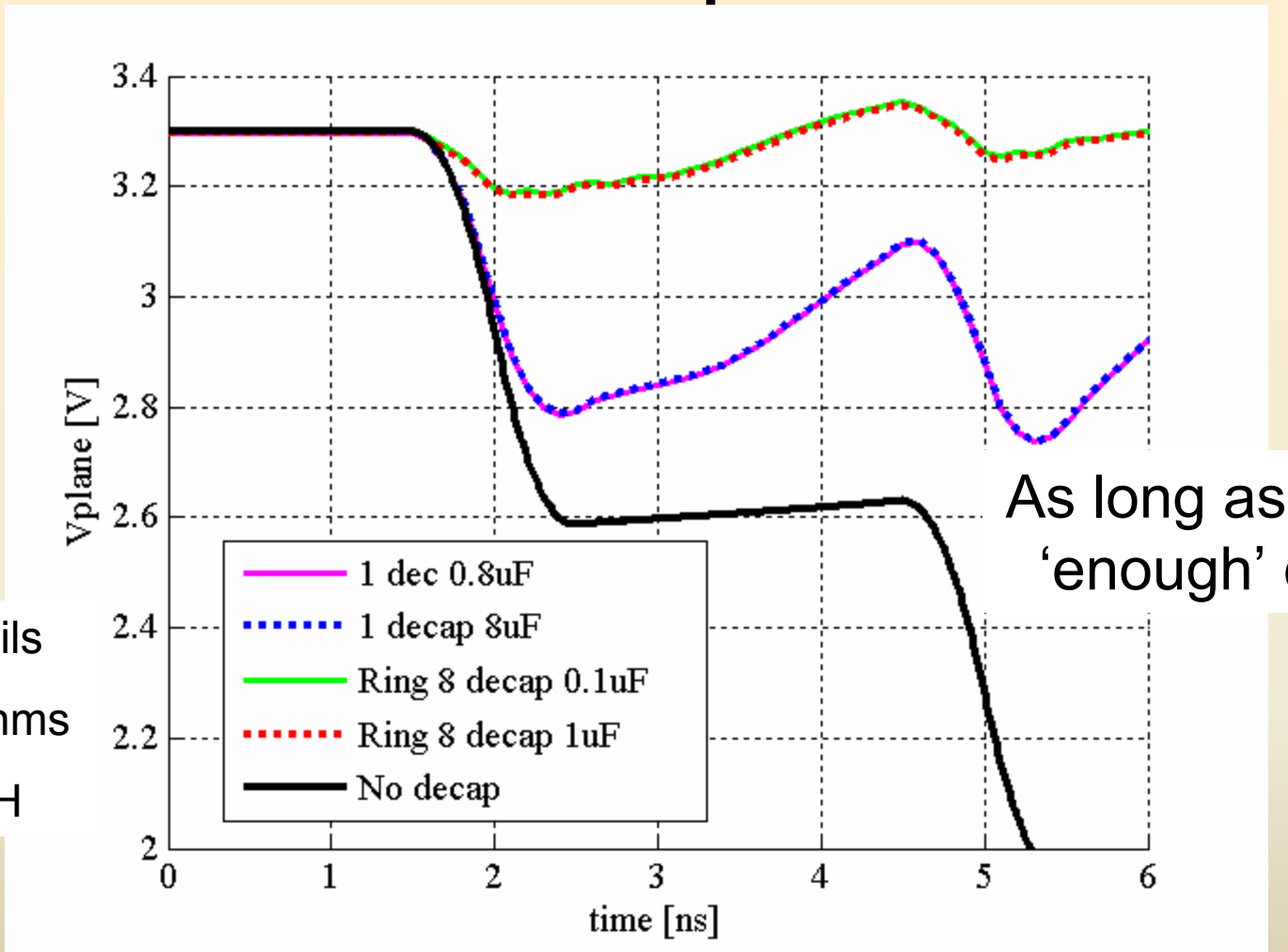
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with 0.5 nH Connection L) with Various Capacitor Values



Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with 1 nH Connection L) with Various Capacitor Values



Noise Voltage is INDEPENDENT of Amount of Capacitance!



As long as there is 'enough' charge

Dist=400 mils

ESR=30mOhms

ESL=0.5nH

Decoupling Summary (1)

- EMC Frequency Domain analysis
  - Steady-state conditions → resonances
  - Transfer function across the board
  - Measurements and simulations agree well
  - Distance of capacitors from ASIC load does not change steady-state impedance

Decoupling Summary (2)

- Charge Delivery Time-Limited analysis
  - Using equivalent SPICE circuit from simulations
  - Current from capacitors change significantly as capacitor moves further away from ASIC
  - Noise at ASIC pins increase significantly as capacitor moves further away from ASIC
  - Steady-state frequency domain analysis not sufficient for charge delivery design of decoupling capacitors

Decoupling Summary (3)

- Recharge the planes
  - Location of Capacitor does matter!
    - Effect more significant for thick dielectrics
  - Connection Inductance is important
  - Value of capacitance not important
  - More capacitors is better than larger/fewer capacitors

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